THREE-PHASE VOLTAGE SOURCE INVERTER WITH VERY HIGH EFFICIENCY BASED ON SiC DEVICES

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M.Sc. Hani Muhsen

ABSTRACT

This dissertation aims at designing a three-phase voltage source inverter based on the SiC devices and mainly the SiC-MOSFET. The designed inverter offers a possibility to drive the power inverter with a very high efficiency, which can reach up to 99% for 16 kW rated power. The design is dedicated to the electric vehicle application, and it aims at

- Providing a comparative study on some of the current discrete SiC devices in terms of the total losses and the thermal conductivity. In addition, a behavioral study of the effective channel mobility with temperature variation in the SiC MOSFET will be investigated.

- Designing a gate driver which fits with the driving requirements of the SiC-MOSFET and provides a trade-off between the switching losses and the EMI behavior.

- Designing a three-phase voltage source inverter with 16 kW rated power; the design includes minimizing the inverter losses and extracts the EMI model of the power inverter by considering the effects of the parasitic parameters; moreover a short guideline for selecting the heat-sink based on the static network is introduced.

- Proposing a new and simplified carried-based PWM, this will reduce the harmonics in the output waveforms and enhance the utilization of the DC-link voltage.

- Proposing a new strategy for compensating the dead-time effect in carrier based-PWM and to find out the proper dead-time level in VSI based on SiC –MOSFET.

- Designing faults diagnosis and protection circuits in order to protect the power inverter from the common faults; overcurrent, short-circuit, overvoltage, and overtemperature faults.
# Nomenclature

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{\text{Gate}}$</td>
<td>Dissipated power by the gate driver</td>
<td>W</td>
</tr>
<tr>
<td>$V_{\text{GGon}}$</td>
<td>Positive gate voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{GGoff}}$</td>
<td>Negative gate voltage</td>
<td>V</td>
</tr>
<tr>
<td>$Q_{\text{gate}}$</td>
<td>Maximum gate charge</td>
<td>C</td>
</tr>
<tr>
<td>$f_{\text{sw}}$</td>
<td>Switching frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>TCP</td>
<td>Temperature Coefficient Point</td>
<td>___</td>
</tr>
<tr>
<td>$I_{GP}$</td>
<td>Peak current of the driver</td>
<td>A</td>
</tr>
<tr>
<td>$R_G$</td>
<td>External gate resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>$R_R$</td>
<td>Internal gate resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>$I_g$</td>
<td>Average gate current</td>
<td>A</td>
</tr>
<tr>
<td>$C_{\text{fin}}$</td>
<td>Input capacitance of SiC-MOSFET</td>
<td>F</td>
</tr>
<tr>
<td>$V_{\text{GS}}$</td>
<td>Gate voltage</td>
<td>V</td>
</tr>
<tr>
<td>$P_{\text{CM}}$</td>
<td>Conduction losses of MOSFET</td>
<td>W</td>
</tr>
<tr>
<td>$I_{\text{on(rms)}}$</td>
<td>On-state rms current of the SiC-MOSFET</td>
<td>A</td>
</tr>
<tr>
<td>$R_{\text{ds(on)}}$</td>
<td>On-state resistance of the SiC-MOSFET</td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{\text{DS(sat)}}$</td>
<td>MOSFET’s voltage drop during on-state</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{DS}}$</td>
<td>MOSFET’s voltage drop</td>
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<tr>
<td>$I_o$</td>
<td>On-state peak current in the SiC-MOSFET</td>
<td>A</td>
</tr>
<tr>
<td>$M$</td>
<td>Modulation index</td>
<td>___</td>
</tr>
<tr>
<td>$\cos \theta$</td>
<td>Power factor</td>
<td>___</td>
</tr>
<tr>
<td>$P_{\text{CD}}$</td>
<td>Conduction losses in Schottky diode</td>
<td>W</td>
</tr>
<tr>
<td>$V_{\text{D}}$</td>
<td>Forward voltage of Schottky diode</td>
<td>V</td>
</tr>
<tr>
<td>$I_{F,\text{avg}}$</td>
<td>Average forward current in Schottky diode</td>
<td>A</td>
</tr>
<tr>
<td>$I_{F,\text{rms}}$</td>
<td>rms forward current in Schottky diode</td>
<td>A</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>------------------------------------------------------------------------------</td>
<td>-------</td>
</tr>
<tr>
<td>R_D</td>
<td>On-state resistance of Schottky diode</td>
<td>Ω</td>
</tr>
<tr>
<td>E_on , E_on,M</td>
<td>Turn-on energy in SiC-MOSFET</td>
<td>J</td>
</tr>
<tr>
<td>V_d(t)</td>
<td>Voltage drop of the Schottky diode as a function of time</td>
<td>V</td>
</tr>
<tr>
<td>I_D, I_Ds, I_d</td>
<td>Drain/ collector current</td>
<td>A</td>
</tr>
<tr>
<td>I_d(t)</td>
<td>Forward current of the Schottky diode as a function of time</td>
<td>A</td>
</tr>
<tr>
<td>E_on,Msi</td>
<td>Turn-on energy of the SiC-MOSFET without the reverse recovery effect</td>
<td>J</td>
</tr>
<tr>
<td>E_on,Mrr</td>
<td>Turn-on energy caused by reverse recovery effect</td>
<td>J</td>
</tr>
<tr>
<td>t_on</td>
<td>Turn-on time</td>
<td>s</td>
</tr>
<tr>
<td>t_off</td>
<td>Turn-off time</td>
<td>s</td>
</tr>
<tr>
<td>dI/dt</td>
<td>Current change rate during switching</td>
<td>A/s</td>
</tr>
<tr>
<td>dV/dt</td>
<td>Voltage change rate during switching</td>
<td>V/s</td>
</tr>
<tr>
<td>t_r</td>
<td>Current rise time during turn-on</td>
<td>s</td>
</tr>
<tr>
<td>t_f</td>
<td>Voltage fall time during turn-on</td>
<td>s</td>
</tr>
<tr>
<td>Q_r</td>
<td>Reverse recovery charge</td>
<td>C</td>
</tr>
<tr>
<td>V_{dc}</td>
<td>Input dc voltage</td>
<td>V</td>
</tr>
<tr>
<td>I_{off (rms)}</td>
<td>Rms current in the SiC device during the turn-off</td>
<td>A</td>
</tr>
<tr>
<td>I_{rms (max)}</td>
<td>Maximum permitted rms current in SiC device</td>
<td>A</td>
</tr>
<tr>
<td>P_{sw,M}</td>
<td>Switching losses of the SiC-MOSFET</td>
<td>W</td>
</tr>
<tr>
<td>t_ru</td>
<td>Voltage rise time in SiC-MOSFET during turn-off</td>
<td>s</td>
</tr>
<tr>
<td>t_fi</td>
<td>Current fall time in SiC-MOSFET during turn-off</td>
<td>s</td>
</tr>
<tr>
<td>E_off, E_off,M</td>
<td>Turn-off energy in SiC-MOSFET</td>
<td>J</td>
</tr>
<tr>
<td>E_onD</td>
<td>Switching energy of the diode</td>
<td>J</td>
</tr>
<tr>
<td>E_Tot</td>
<td>Total Energy losses</td>
<td>J</td>
</tr>
<tr>
<td>i_F(t)</td>
<td>Forward current in the Schottky diode as a function of time</td>
<td>A</td>
</tr>
<tr>
<td>V_F(t)</td>
<td>Forward voltage drop of Schottky diode as a function of time</td>
<td>V</td>
</tr>
<tr>
<td>P_onD</td>
<td>Switching losses of the Schottky diode</td>
<td>W</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>------</td>
</tr>
<tr>
<td>$C_{dc-link}$</td>
<td>DC-link capacitance</td>
<td>$F$</td>
</tr>
<tr>
<td>$I_{d,\text{rms}}$</td>
<td>Rms current in the DC-link</td>
<td>$A$</td>
</tr>
<tr>
<td>$I_{d,\text{dc}}$</td>
<td>Average current in the DC-link</td>
<td>$A$</td>
</tr>
<tr>
<td>$T_j, T_{j,MOSx}$</td>
<td>Junction temperature of the SiC-MOSFET</td>
<td>°C</td>
</tr>
<tr>
<td>$T_a$</td>
<td>Ambient temperature</td>
<td>°C</td>
</tr>
<tr>
<td>$P_{\text{MOSFET}x}$</td>
<td>Total losses in SiC-MOSFET number $x$</td>
<td>$W$</td>
</tr>
<tr>
<td>$R_{\text{jc,MOS}x}$</td>
<td>Junction to case thermal resistance of MOSFET number $x$</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\text{cs,MOS}x}$</td>
<td>Case to sink case thermal resistance of MOSFET number $x$</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\text{ca}}$</td>
<td>Case to ambient thermal resistance</td>
<td>°C/W</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse width modulation</td>
<td>—</td>
</tr>
<tr>
<td>$\Delta T_{ca}$</td>
<td>Temperature difference between the case and the sink</td>
<td>°C</td>
</tr>
<tr>
<td>$\Delta T_{ja}$</td>
<td>Temperature difference between the junction and the ambient</td>
<td>°C</td>
</tr>
<tr>
<td>$V_{\text{trigger}}$</td>
<td>Trigger voltage to send deactivation trigger signal</td>
<td>$V$</td>
</tr>
<tr>
<td>$C_s$</td>
<td>Stray capacitance per unit length of the drain plate</td>
<td>$F/m$</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>Relative permittivity</td>
<td>—</td>
</tr>
<tr>
<td>$\varepsilon_\infty$</td>
<td>Free space permittivity</td>
<td>$F/m$</td>
</tr>
<tr>
<td>$L$</td>
<td>Length</td>
<td>$m$</td>
</tr>
<tr>
<td>$W$</td>
<td>Width</td>
<td>$m$</td>
</tr>
<tr>
<td>$H$</td>
<td>The distance between the drain plate and the heat-sink</td>
<td>$m$</td>
</tr>
<tr>
<td>$T$</td>
<td>Drain plate thickness</td>
<td>$m$</td>
</tr>
<tr>
<td>$S$</td>
<td>Separation distance between the adjacent drain plates</td>
<td>$m$</td>
</tr>
<tr>
<td>$C_{h-g}$</td>
<td>Stray capacitance between the ground and the heat-sink</td>
<td>$F$</td>
</tr>
<tr>
<td>$A$</td>
<td>The area of the top side of the heat-sink</td>
<td>$m$</td>
</tr>
<tr>
<td>$d$</td>
<td>Separation distance between the heat-sink and the ground</td>
<td>$m$</td>
</tr>
<tr>
<td>$C_{h-t}$</td>
<td>Total heat-sink stray capacitance</td>
<td>$F$</td>
</tr>
<tr>
<td>$V_{an}$</td>
<td>The phase to neutral voltage of phase a</td>
<td>$V$</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>------</td>
</tr>
<tr>
<td>( V_{ba} )</td>
<td>The phase to neutral voltage of phase b</td>
<td>V</td>
</tr>
<tr>
<td>( V_{ca} )</td>
<td>The phase to neutral voltage of phase c</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\alpha} )</td>
<td>( \alpha )-voltage (transformed voltage)</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\beta} )</td>
<td>( \beta )-voltage (transformed voltage)</td>
<td>V</td>
</tr>
<tr>
<td>( \omega_t )</td>
<td>The phase voltage angle</td>
<td>rad</td>
</tr>
<tr>
<td>A</td>
<td>Voltage formula abbreviation for phase A</td>
<td>V</td>
</tr>
<tr>
<td>B</td>
<td>Voltage formula abbreviation for phase B</td>
<td>V</td>
</tr>
<tr>
<td>C</td>
<td>Voltage formula abbreviation for phase C</td>
<td>V</td>
</tr>
<tr>
<td>Quad( _x )</td>
<td>Quadrant number ( x ); ( x=1,2,3,4 )</td>
<td>___</td>
</tr>
<tr>
<td>Sec( _x )</td>
<td>Sector number ( x ); ( x=1,2,\ldots,6 )</td>
<td>___</td>
</tr>
<tr>
<td>( T_{x,\text{pulse}} )</td>
<td>The pulse width of phase ( x ); ( x=a,b,c )</td>
<td>s</td>
</tr>
<tr>
<td>( T_{sw} )</td>
<td>Switching period time</td>
<td>s</td>
</tr>
<tr>
<td>( T_{x,\text{off}} )</td>
<td>Turn-off time of phase ( x ); ( x=a,b,c )</td>
<td>s</td>
</tr>
<tr>
<td>( T_{xon} )</td>
<td>Turn-on time of phase ( x ); ( x=a,b,c )</td>
<td>s</td>
</tr>
<tr>
<td>( V_{dc} )</td>
<td>DC-Link voltage</td>
<td>V</td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion</td>
<td>___</td>
</tr>
<tr>
<td>( L_{ch} )</td>
<td>Radial Channel length</td>
<td>m</td>
</tr>
<tr>
<td>( W_{ch} )</td>
<td>Mean channel width</td>
<td>m</td>
</tr>
<tr>
<td>( C_{ox} )</td>
<td>Oxide capacitance per unit area</td>
<td>F/m(^2)</td>
</tr>
<tr>
<td>( V_t )</td>
<td>Charge threshold voltage</td>
<td>V</td>
</tr>
<tr>
<td>( \mu_{\text{eff}} )</td>
<td>Effective channel mobility</td>
<td>m(^2)/V.s</td>
</tr>
<tr>
<td>( \theta )</td>
<td>Mobility reduction factor</td>
<td>1/V</td>
</tr>
<tr>
<td>( \mu_0 )</td>
<td>Low field mobility</td>
<td>m(^2)/V.s</td>
</tr>
<tr>
<td>( g_{mn} )</td>
<td>Transconductance</td>
<td>S</td>
</tr>
<tr>
<td>( V_d )</td>
<td>Drain voltage</td>
<td>V</td>
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1. Introduction

1.1. Background

Power electronic devices are playing a significant role in different aspects of electrical systems and their applications, and they have gone through several improvement phases in the last decades in terms of their features and applications. One of the important power circuits, which can be found in many applications, is the power inverter which converts the DC waveform to an AC waveform. The power inverter can be found in several applications such as the adjustable speed drive (ASD), the uninterruptible power supply (UPS), as well as in flexible AC transmission.

The design of the power inverter can be affected by several control factors, such as the selected power devices, switching frequency, the electromagnetic interference (EMI) and the thermal behavior of the power devices. Some years ago, the Si was the main material forming the semiconductor power devices which have been employed in power electronics application. For instance, the Si-BJT was employed at high current densities due to its low forward voltage drop. On the other hand, the driving of the Si-BJT was nontrivial beside the high driving losses in
contrast to the unipolar devices. Moreover, Si-BJT exhibited low switching speed capabilities. Therefore, the trends in power electronics applications within the medium voltage range were directed towards the utilization of the Si-MOSFET due to its simplicity of control and its high switching capability, i.e. up to a few MHz. One of the challenges in front of the utilization of the Si-MOSFET was its low current conductivity.

For the sake of combining the benefits of the BJT and the Si-MOSFET, the IGBT was proposed with a MOSFET gate structure and output structure of the BJT in order to cover a higher voltage range. The utilization of the IGBT was faced with several problems: one problem was the tail current during the turn-off, which is the main responsible factor of the high switching losses in the IGBT in addition to its influence on limiting its maximum switching speed to 20 kHz. This current behavior is resulted from the combination of the minority carrier in the drift layer of the IGBT which can reach to several microseconds and it is correlated with the blocking voltage of the IGBT.

The launch of the IGBT was the reason to abandon the BJT and the MOSFET for voltages higher than 600V for most of the power electronics applications due to its control simplicity, the capability of operating with adequate switching speeds and its higher rated voltage levels. Despite the benefits of the Si-IGBT in the medium voltage range, its application efficiency is still the main challenge. Therefore, the ambition in the last years towards the utilization of power semiconductor devices that are capable of working at higher-temperature levels and lower losses, smaller filter size and cooling systems in different power electronics fields such as electric vehicle applications, were the reasons to introduce the wide-band gap materials such as SiC, GaAs and GaN materials as alternatives to the Si-technology.

The SiC-technology is considered as a promising solution for fabricating power devices, due to its ability to push up the maximum junction temperature and the breakdown-voltage levels over the Si limits. Theoretically, the SiC material can sustain up to 600 °C, which is five times higher than Si. Despite of the SiC material capability to sustain higher temperature levels, this benefit is still not applicable due to the limitation of the packaging technology. SiC devices are expected to be rated for higher blocking voltages than Si; these levels can reach up to ten times higher [1]. Moreover, they have a smaller chip size and a thinner space charge width in comparison with the
Si devices. This leads to moderate internal capacitances in the SiC devices and low gate charge in case of the unipolar devices.

In addition to the previous benefits, SiC devices are superior in terms of the thermal conductivity, which is three times higher than that of their rivals; this will lead to a scaling down of the size of the cooling system. On the other hand, there are still several challenges against the wide spread of SiC devices, such as the high prices of SiC devices, the low current and voltage ratings in comparison with Si devices and the oscillation behavior during the switching transition. SiC devices are expected to become less expensive in the power electronics market in the forthcoming decade, making them the affirmed alternatives to the Si devices in many applications especially in the medium voltage range.

1.2. Fundamentals of SiC Devices

Recently, several SiC devices are commercially available in power electronics markets. These devices can be considered in a certain way as devices under investigation for the sake of proving their reliability beside their promised efficiency and they can be classified into two types based on charge carriers. The first type is the unipolar transistor, the resulted current in these devices depend on only one type of charge carriers (majority carriers). The second type is the bipolar transistor, in which the current is formed based on two charge carriers, i.e. the holes and the electrons.

In this work, a study of some feasible SiC devices in the power electronics market will be accomplished. The study attempts to highlight the aforementioned types of power transistors in the SiC Technology; the investigated unipolar transistors were a different generation of SiC MOSFETs, while the investigated bipolar transistor was the SiC BJT. Moreover, this work aims at showing the benefits and the capabilities of each type. The comparison between the investigated devices will be addressed with regard to five parameters. First, an overview of the physical structure and the fabrication of the SiC MOSFET and bipolar SiC device (SiC-BJT) will be introduced; followed by a comparison of the switching losses relying on theDatasheet parameters as a preliminary study.
Third, the maximum allowable dissipated power of the devices under study, the conduction losses and the thermal conductivity will also be presented. Fourth, the driving complexity of the two types will be discussed with regard to the design simplicity and efforts. It is worth mentioning that the SiC JFET was excluded from this comparison due to the abundance of works about these devices, presenting their benefits and capabilities as will be shown in the next section. Finally, the chip size of the investigated devices will be compared to obtain a rough idea about the chip size in each single device.

1.2.1. The Physical Structures of the SiC MOSFET and the SiC BJT

The common physical structure of the second generation of the SiC MOSFETs in modern power electronics is the planar double-implanted MOSFETs in 4H-SiC. This label came from the doping profiles in SiC DMOS transistors, which must be defined by consecutive implantation in the base region by aluminum or boron and in the source region by the nitrogen or phosphorus. This structure consists of the horizontal inversion channel beneath the gate oxide and the vertical channel which forms the JFET region between the two p-well regions as shown in Figure 1.1. The benefits of this dual structure can be summarized in the high blocking voltage capability in addition to the resulted low on-state resistance. Figure 1.1 shows the cell structure of the second generation of the SiC MOSFETs according to [3].

The fabrication of the SiC MOSFET is performed by implanting the surface of the semiconductor with the diffused n+ and the p+ implantations; these regions are connected to the source metallization. Moreover, the p wells and the channels are separated from the gate metallization which is formed by a heavily doped n poly-Si, by the gate dielectric which is formed from SiO2 and it has a dielectric permittivity of 3.9.

The n+ layer is grown epitaxially over n+ SiC substrate, which will form the drift layer; these configurations will be mounted afterwards in a planar SiC-face structure. In order to form the channel current; a positive gate voltage must be applied at the gate contact to induce the majority carriers to flow from the diffused n+ through the horizontal inversion layers to the p wells. If the applied gate voltage is increased higher than the threshold voltage, the current will flow through the vertical JFET in the drift region and then to the n+ SiC substrate; and finally, the
current will arrive at the drain contact while the current through the body diode will flow directly from the p-well to the drift layer as shown in Figure 1.1.

One of the demands for the sake of reducing the on-state resistance in the SiC MOSFET is the mitigation of the resistances of the JFET regions. Although several works discussed the dominance contribution of the channel resistance in contrast to the other regions as in [2], the mitigation of the JFET resistance is still expected to benefit from the final on-state resistance. Recently, ROHM Company has announced the production of the third generation of the SiC MOSFET, which has a double trench structure. This label comes from the extra trench on the source side additional to the former trench MOSFET. The cell structure of the conventional trench MOSFET and the third generation of the SiC MOSFET [3] are depicted in Figure 1.2 (a) and (b).

![Figure 1.1: Cell structures of the second generation of SiC MOSFET according to [3].](image)

This enhancement is expected to reduce the possible degradation in the gate oxide due to the mitigation of the high electric field in the drift region by distributing the electric field to source sides. Moreover, this technology is expected to reduce the on-state resistance up to 50% (40 mΩ for 1.2KV) in contrast to the second generation (80 mΩ for 1.2KV).

This reduction results from the absence of the JFET resistance in this generation. In addition to the reduced switching losses, which is expected to become 30% lower than the second generation. This structure is expected to enhance the switching speed capabilities due to the
reduction of the input capacitance ($C_{iss}$). This reduction can reach up to 70% of the same chip size. Despite the claimed benefits of the third-generation SiC MOSFET, the reliability of these devices is still under investigation. On the other side, the third-generation of CREE SiC-MOSFETs settles on the same structure and more efforts have been made to optimize and reduce the size of the die structure [4].

Figure 1.2: (a) Ordinary single trench MOSFET (left), the third generation of ROHM SiC MOSFET (right) according to [5].

The SiC BJT can be classified into two different types based on the fabrication approaches. The first one is known as an implanted emitter in SiC BJT. In this type, the emitter is formed by implanting the phosphorus ions for NPN SiC BJT into the n epilayer in order to form the implanted n$^+$ emitter above the p$^-$ epilayer, which is connected with the emitter contact. Similarly, the base is formed by a grown p$^+$ epilayer, which is connected by the base metallization and finally the previous epilayers were grown on the n$^-$ collector epilayer as depicted in Figure 1.3 (a). The second type is the epitaxial emitter BJT in this fabrication approach; the n$^+$ epilayer is grown epitaxially to form the emitter, while the p$^+$ epilayer is implanted in the p$^-$ epilayer as depicted in Figure 1.3 (b).
The epitaxial SiC BJT offers higher levels of current gain in contrast to the implanted emitter SiC BJT. In addition, the epitaxial SiC BJT shows simplicity in structure and in the fabrication processes. This imperfection in the implanted emitter SiC BJT returns to the high implant induced defects in the base and emitter carriers, which usually result in reducing the emitter injection efficiency [6].

1.2.2. An Evaluation of SiC MOSFETs and SiC BJT

The evaluation in this part will include some samples, which belong to the different power switch groups. The first component, which belongs to the unipolar group, is the ROHM SiC-MOSFET with product number SCH2080KE, a breakdown voltage of 1.2 kV, a maximum rated current of 35 A and a maximum junction temperature of 150 °C. This device represents the main component in the constructed three-phase inverter prototype in this work.

The second component, which belongs to the identical type, is the second generation of CREE SiC-MOSFET with the product number C2M0080120D, which is rated to 1.2 kV and 35 A. The last component in the same group is the first generation of CREE SiC MOSFET (CMF20120D), which is rated for a continuous current 42 A at room temperature and at a gate voltage of 20 V. All the examined devices were limited to a breakdown voltage of 1.2 kV. On the other side, the NPN SiC BJT with the product number FSICBH017A120 is manufactured by Fairchild with a rated breakdown voltage of 1.2 kV and 50 A as rated current. The FSICBH017A120 has a
maximum junction temperature of 175 °C. The electrical specifications of the investigated devices have been summarized in Table 1.1.

Primarily, the switching energy losses have been extracted for the four devices based on the manufacturer datasheets. Despite the fact that the comparison was made at similar test conditions, the outcomes still showed superiority for the SCH2080KE in terms of the turn-off and turn-on losses. SCH2080KE showed turn-off and turn-on energy losses of 64 µJ and 218 µJ, respectively. These values have been compiled at a DC-link voltage of 600 V with a drain current of 10 A; the considered external gate resistance has been assumed zero Ω. The turn-off and turn-on energy losses of the devices under study are summarized in Table 1.1.

<table>
<thead>
<tr>
<th>Device</th>
<th>Measurement Conditions</th>
<th>V GS or I B</th>
<th>E off, E on</th>
<th>R G</th>
<th>Temp.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROHM MOSFET SCH2080KE</td>
<td>800 V/10 A L=500 µH includes diode reverse recovery</td>
<td>18V/0V</td>
<td>100 µJ , 365 µJ</td>
<td>0 Ω</td>
<td></td>
</tr>
<tr>
<td>Fairchild NPN BJT FSICBH017A120</td>
<td>800 V/20 A I B On and Off Peak=6 A I BE On Static =1.5 A</td>
<td>18V/0V</td>
<td>210 µJ , 351 µJ</td>
<td></td>
<td>150 °C</td>
</tr>
<tr>
<td>CREE MOSFET C2M0080120D</td>
<td>800 V/20 A L=142 µH</td>
<td>20V/-5V</td>
<td>135 µJ , 265 µJ</td>
<td>2.5 Ω</td>
<td></td>
</tr>
<tr>
<td>CREE Z-FET™ MOSFET CMF20120D</td>
<td>800 V/20A L=865 µH</td>
<td>20V/0V</td>
<td>310 µJ , 310 µJ</td>
<td>7.5 Ω</td>
<td></td>
</tr>
</tbody>
</table>

Table 1.1: Comparison of turn-off and turn-on energies extracted from the double pulse test results based on the datasheets

Furthermore, the total switching losses of the investigated devices at abutting ratings have been summarized in Table 1.2. SCH2080KE again presents superiority over the other devices, which means that its ability of enhancing the system efficiency at higher switching speeds are requested. Switching losses are not the only parameters which affect the system efficiency, but also the conduction losses, which are considered as the dominant source of losses in the power converters such as the three-phase inverter. The necessity to consider these types of losses, especially in some applications as in the electric vehicle, returns to the limitation of energy.
sources, i.e. the battery. Therefore, the selection of the SiC device should consider the device with the minimum conduction losses and the best switching behavior.

Each power device has a capability to dissipate a specific level of power losses without cooling requirements and this level is known as the maximum allowable dissipated power. These levels of the investigated devices with elevated junction temperatures have been analyzed and depicted in Figure 1.4. Moreover, the comparison was addressing the conduction losses in the investigated devices, where FSICBH017A120 revealed the lowest on-state resistance in contrast to SCH2080KE and C2M0080120D. In fact, the mentioned SiC-MOSFETs showed similarities in terms of the conduction losses at room temperature and lower conduction losses in the favor of the C2M0080120D at higher junction temperatures. This means that FSICBH017A120 has the highest capability to dissipate the power at elevated temperatures in contrast to the other devices as depicted in Figure 1.4.

On the other hand, the environment temperature is playing a prominent role in increasing the device losses. Therefore, the devices with the highest maximum junction temperature and the proper thermal junction-to-case resistance should be considered in order to reduce the cooling requirements in the different applications in which the system’s size is a dominant design parameter as in the electric vehicle. The values of the maximum junction temperature and the thermal junction-to-case resistance of the four devices have been discharged in Table 1.3.

<table>
<thead>
<tr>
<th>Device</th>
<th>( E_{\text{off}} )</th>
<th>( E_{\text{on}} )</th>
<th>( E_{\text{Tot}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROHM MOSFET SCH2080KE</td>
<td>100 ( \mu )J</td>
<td>365 ( \mu )J</td>
<td>465 ( \mu )J at ( I_D = 10 ) A</td>
</tr>
<tr>
<td>Fairchild NPN BJT FSICBH017A120</td>
<td>210 ( \mu )J</td>
<td>351 ( \mu )J</td>
<td>561 ( \mu )J at ( I_D = 20 ) A</td>
</tr>
<tr>
<td>CREE Z-FET\text{TM} MOSFET C2M0080120D</td>
<td>135 ( \mu )J</td>
<td>265 ( \mu )J</td>
<td>400 ( \mu )J at ( I_D = 20 ) A</td>
</tr>
<tr>
<td>CREE Z-FET\text{TM} MOSFET CMF20120D</td>
<td>310 ( \mu )J</td>
<td>310 ( \mu )J</td>
<td>620 ( \mu )J at ( I_D = 20 ) A</td>
</tr>
</tbody>
</table>

Table 1.2: Total energy losses based on the manufacturer datasheet for inductive loads

The next step of the comparison process is investigating the driving complexity of the devices under study. For instance, the BJT is considered as a current driven device, which requires applying a continuous base current to ensure a constant collector current during the conduction-state. The design of the BJT driver has to comprise the safe startup circuit to avoid the hazards of the high turn-on current, which can result in destroying the driven devices. Additionally, the
existence of protection circuits is a crucial issue, which should also be taken into account during the design phase.

The difficulty of achieving the driving requirements of the SiC BJTs in contrast to SiC-MOSFET prompted the SiC-MOSFET to be the preferred selection of this work as well as in modern power electronics due to its lower driving requirements and control simplicity. The MOSFET is known as a voltage controlled device which requires a constant voltage to be applied to its gate; this voltage should remain higher than the threshold gate voltage at the gate terminal during the conduction-state to keep the MOSFET in the conduction mode.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Type</th>
<th>Max. Junction Temp.</th>
<th>Max. R thermal, Junction-case</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCH2080KE</td>
<td>MOSFET</td>
<td>175 °C</td>
<td>0.44 °C/W</td>
</tr>
<tr>
<td>FSICBH017A120</td>
<td>BJT</td>
<td>175 °C</td>
<td>0.45 °C/W</td>
</tr>
<tr>
<td>C2M0080120D</td>
<td>MOSFET</td>
<td>150 °C</td>
<td>0.65 °C/W</td>
</tr>
<tr>
<td>CMF20120D</td>
<td>MOSFET</td>
<td>135 °C</td>
<td>0.51 °C/W</td>
</tr>
</tbody>
</table>

Table 1.3: Maximum junction temperatures and thermal resistances of SiC transistors with TO-247 packages

The purely capacitive gate of the MOSFET led to consider it as a benefit for the SiC MOSFET in contrast to its counterpart (BJT), which means providing a current through the gate during the steady state is inessential. On the other hand, the driver of the MOSFET should be able to provide high current and low impedance at the gate during the transition time in order to inject and remove the charges of the input capacitance and the included Miller capacitances owing to the effects of those capacitances in limiting the switching speed of the power devices.
As the comparison of the dimensions of the active areas for the investigated devices is hard to achieve due to their unavailability from the manufacturers, the die sizes will be conducted instead. In [7] and [8], the normalized die sizes of investigated SiC devices in relative to the die size of the C2M0080120D have been reported. This relation can be exploited to extract the die size of the CMF20120D, which was unavailable during the die sizes measurements. Accordingly, the die size value of the C2M0080120D was measured and it has been multiplied by the normalization factor of the CMF20120D. It is worth mentioning that the die sizes measurements of the SCH2080KE, FSICBH017A120 and C2M0080120D have been collected by the Scanning Acoustic Microscope (SAM). Finally, the die sizes of the investigated devices have been discharged in Table 1.4.

<table>
<thead>
<tr>
<th>The Device</th>
<th>The Die Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCH2080KE</td>
<td>0.172 cm²</td>
</tr>
<tr>
<td>FSICBH017A120</td>
<td>0.185 cm²</td>
</tr>
<tr>
<td>C2M0080120D</td>
<td>0.104 cm²</td>
</tr>
<tr>
<td>CMF20120D</td>
<td>0.165 cm²</td>
</tr>
</tbody>
</table>

Table 1.4: The die sizes of the investigated devices by using Scanning Acoustic Microscope.

In this work, the SiC-MOSFET SCH2080KE will be used as the basic component in the three-phase inverter due to its expected low switching loss levels, moderate conduction losses and a low thermal resistance as shown previously throughout this preliminary study and the final results in this work will show its performance in three-phase inverter applications.
1.3. State of Art and Motivations of the Work

In the last decade, the utilization of the SiC devices as an alternative to Si-devices has been highlighted due to the promising features in terms of their higher operating temperature capabilities and the expected high efficiency in various applications, in which the size, cost and better performance are required. The expected benefits of the SiC-technology were not limited to enhance the system efficiency, but also in terms of operating the SiC-devices at high temperatures, which can now reach close to 300 °C for discrete devices with zero conduction current due to the limitations on the packaging technology. On the other hand, the reliability of the SiC devices is still in its infancy.

Electric vehicles (EV) and hybrid-electric vehicles (HEV) applications are expected to be beneficiaries from this involvement. The promising impacts of the SiC-technology will lead to an increase in the efficiency and in the power density of the converters; therefore the cost is expected to be reduced after the technology has matured. The expected efficiency due the utilization of the SiC-technology can extent to very high levels according to [9]. The practice of the SiC-technology is not fully matured until the days of writing this work, the reliability is still under investigation in order guarantee the ability of this technology to be a surrogate to the Si-technology in different disciplines [1]. Hence, the results of this dissertation can be considered as reinforcement for the benefits of the SiC-technology in three-phase inverter applications in terms of the expected very high efficiency levels, which cannot be obtained by the Si-technology without much effort. In addition, the research focused on the requirements of the behavior of the SiC devices. The prior efforts to involve the SiC-devices in three-phase inverter applications will briefly be presented through this section.

The implementation of the SiC devices in three-phase inverters has been started after the production of 4H-SiC-SBD, which was proposed to replace the Si-SBDs to reduce the switching losses. This reduction returns to the low reverse recovery charge in SiC-SBD in contrast to the Si-pin diode, which can reach up to 70% [9]. The minimization of the switching losses was leading to increase the system efficiency and reducing the heat-sink size for low switching speed up to 10 kHz; the benefits of this replacement have been reported in [10] and [11]. This combination between the Si power switches and the SiC SBDs is known as a hybrid-combination, which led to total efficiency levels higher than 90% according to [12].
In the initial production phases, the utilization of the SiC devices was mainly focused on the usage of the SiC-JFET. This returns to the small on-state resistance and the low energy losses of the SiC-JFET, which could enable high switching speeds. In addition, the SiC-JFET has a rugged structure and it does not suffer from degradation problems as in the other SiC devices. Therefore, the SiC-JFET was used in three-phase inverter applications, which require high efficiency, such as the PV inverter. The efficiency improvement which resulted from this utilization in three-phase inverters has been analytically presented in [13].

On the empirical side, the benefits of the SiC-JFET utilization have been discussed in several works as in [14], [15], [16], [17], [18] and [19]. The SiC-JFET struggled with the increased switching losses which accompany the high switching speeds, but this increment can be negligible when it is compared with the reduced conduction losses up to a specific switching frequency.

Moreover, the driving complexity of the SiC-JFET is considered as one of its drawbacks in contrast to the other Si and the later SiC-devices. The driving of the SiC-JFET requires a proper gate driver design to drive the SiC-JFET within the safe operating area in addition to some restrictions on the average gate current; these requirements and more have been addressed in [20], in addition to the enhanced efficiency which resulted from the usage of the SiC-JFET. The employment of the SiC-JFET in the three-phase inverter showed a reduction on the converter size due to the lower cooling and filtering requirements.

The SiC-JFET confirmed its capability to operate in a high-power density inverter with the minimal size and cost and it fulfilled the design requirements. The size reduction can reach up to 70% in the three-phase inverter with a rated power of 100 kW as claimed in [21]. The switching losses represent the lowest portion of the losses in the SiC-inverters, but it might become critical at high switching speed levels, when the switching losses will increase dramatically. This increment will powerfully affect the total losses, hence it will reduce the required efficiency.

Indeed, the switching speed in the three-phase inverter is dependent on the applications. For instance, in the PV-inverters, the high switching frequency will lead to a reduction of the filter size and the total cost, but this is escorted by increasing the heat-sink’s size. Therefore, the inverter design should consider the tradeoff between the system size and its efficiency. The proportional
relation between the switching losses and the switching speed led to produce special SiC-chips which can deal with this issue; further details related to this case can be found in [22].

The on-state resistance is considered as a dominant contributor of the total losses in the three-phase inverter. In fact, this would be true if the switching speed was limited to a certain level. In the literature, the on-state losses are known as the conduction losses, which are dependent on the applied input voltage and the junction temperature. If SiC devices are used as positive temperature coefficient (PTC) devices, their conduction losses are expected to become higher at high temperature levels. Thanks to the PTC behavior of the SiC devices, the parallel configuration becomes possible and it is employed to reduce the effect of the temperature on the on-state losses.

The use of the parallel configuration of the SiC-JFET has been discussed in the literature, see [23]; the results showed the benefits of the configuration in terms of improving the inverter efficiency and enhancing the thermal behavior. On the other hand, the parallel configuration revealed some drawbacks, such as the increased size and cost, which makes the utilization of the configuration dependent on the applications and involves a compromise between the system size and the efficiency.

The cooling methods which have been discussed in the literature and related to the SiC-inverter are dependent on the application and the rated power of the inverter. Some of the previous works showed the possibility of using the natural convection systems as in [24], whereas some works showed the requirement to employ the forced-air cooling technology in order to achieve the required temperature levels in the power circuit which should not exceed the maximum junction temperature of the used SiC devices. One of the proposed methods for reducing the size of the cooling system was the utilization of the parallel configuration in the SiC-inverters which was leading to reduce the conduction losses in the inverter, hence decreasing the size of the heat-sink as in [25]. Considering the parallel configuration, the compiled efficiency in such systems can reach up to 99.5% in 40 kVA three-phase inverters according to [26]. The utilization of the power modules was also one of the proposed solutions to reduce the heat-sink size in the SiC-inverters, see [24].
Before 2009, most of the explored SiC devices in three-phase inverter were discrete samples, which were in the analytical investigation and validation phase as in case of the SiC-JFET, while other SiC-devices have been produced after 2011. The SiC power modules produced before that date were not involved in the inverter design, only some samples of these modules have been investigated in order to highlight the benefits of the SiC-technology. One of the investigated samples in the literature consisted of three SiC-JFETs with rated values 1.2kV/10A for each involved SiC-JFET within the module and these modules have been used to construct a three-phase inverter with a rated power of 18 kW, see [27].

The usage of the power modules revealed a high efficiency around 98%. On the other hand, the modules were suffering from the limitations of the packaging technology, which was still in its infancy back then. SiC power modules have been released to obtain higher efficiency, especially with high power rated three-phase inverters due to their low parasitic inductances, which have been optimized to meet the application requirements.

The SiC-JFET was the first commercial SiC device, which led to mature its power modules before the other SiC devices which have been released later. The benefits of this technology have been tested based on the six-pack JFET, which resulted in increasing the system efficiency up to 98.5% due to the low conduction losses. Furthermore, the switching losses were enhanced due to the restriction on the parasitic parameters effect which can destroy the switching behavior. Further details related to the utilization of the six-pack power module technology in three-phase inverters and its benefits have been discussed in [28].

One of the challenging issues in the three-phase inverter systems is the total cost; especially when the design is made for civilian applications, such as the PV-inverters and EV and Hybrid vehicles, etc., then the cost becomes a major concern that must be taken into consideration. Therefore, the SiC-MOSFET has been introduced in the first place to replace the Si-IGBT. The SiC-MOSFET showed low on-state resistance, faster switching speed and reduced switching losses in contrast to the Si-IGBT which suffers from the tail current during the switching transition limiting its switching capability to 20 kHz. The first SiC-MOSFET was produced by CREE in 2011; nowadays, several power electronics companies produce the SiC-MOSFET and they propose it as a replacement to the IGBT in applications which require discrete devices with rated value 1.2kV/up to 50A.
The attractive feature of the SiC-MOSFET and its ability to switch with higher speeds than other SiC devices, opens the door to comprise the SiC-MOSFET in PV-inverters [29] and in other applications, such as the EV and HEV in which the efficiency and the switching speed in addition to the system size represent the design parameters that must be fulfilled. It is expected that the annual costs and the long-term costs of the PV-inverter become less expensive if the Si-IGBT has been replaced by the SiC-MOSFET and it is expected to obtain an enhancement of the system efficiency, which can reach up to 98% according to [30].

The usage of the SiC-MOSFET in the three-phase inverter in PV-inverter has been discussed for the first time in [13] and it also included a comparative study which highlighted the superiority of SiC-MOSFET over the Si-IGBT. The results showed a 2% enhancement on the total system efficiency. The samples of the SiC-MOSFET which have been used in [31] were regarded as the first discrete SiC-MOSFET samples produced by CREE, the used samples were under investigation before the release of the commercial samples. Moreover, the superiority of the SiC-MOSFET over the Si MOSFET and the gained benefits of employing the SiC-MOSFET in the induction heat inverter have been discussed in [32].

The SiC-MOSFET power modules and their benefits in terms of increasing the system efficiency have been investigated in [33]; the results were promising and they showed the ability of the SiC-MOSFET power modules to achieve high system efficiency up to 99.3% in motor drive applications. Finally, the SiC-MOSFET is expected to replace the Si-IGBT in the coming years due to the following features which have been investigated in [34]:

- The IGBT is considered as a minority carrier device, which means that the injection of the minority carrier is necessary in order to control the on-state resistance, whereas the SiC-MOSFET is showing a much lower on-state, which will result in reducing the conduction losses.

- The switching speed of the IGBT in the literature was limited to 20 kHz, which restricts its usage in various applications in which the fast switching speed is a major concern. On the contrary, the switching speed in the SiC-MOSFET can extend to higher switching speeds up to several hundred kHz.
The utilization of SiC-MOSFET showed lower switching losses than the IGBT, especially regarding the turn-off losses.

The filtering requirements of the IGBT are higher than the filtering requirements in case of the SiC-MOSFET in terms of the passive components.

The features of SiC-MOSFET resulted in smaller chip sizes, minor gate capacitances and smaller total gate charges. These features were leading to reduce the switching losses in SiC-MOSFETs in comparison with IGBT.

The Si-IGBT was rated in the literature from 500 V and up to 6.5 kV, whereas the discrete SiC-MOSFET was rated from 600V and up to 5 kV (theoretically) and practically from 600V up to 1.7 kV until the date of writing this work.

The utilization of the SiC-MOSFET in the three-phase inverter also has several benefits over the utilization of the Si-MOSFET. These benefits have been reported throughout the literature and they can be summarized by the following points:

- The SiC-MOSFET has a lower on-state resistance than the Si-MOSFET with the same breakdown voltage and identical ratings.
- Higher switching speeds and lower switching losses can be obtained by using SiC-MOSFET.
- The chip size of SiC-MOSFET is smaller than the Si-MOSFET with the same ratings.
- New and higher breakdown voltage ranges became available by introducing the SiC-MOSFET, which can be considered as inaccessible levels by the Si-MOSFET.
- The SiC-MOSFET showed lower reverse recovery charges of the integrated body diode in contrast to the Si-MOSFET.

One of the common problems associated to SiC devices is the effect of the parasitic parameters which cause oscillations during the switching transitions. These oscillations have an impact on the switching behavior and they increase the switching losses. Additionally, the conducted EMI and the radiated EMI are expected to become higher due to the generated oscillations. Some of the previous works recommended a good layout of the gate driver and to place it as close as possible to the gate terminal in order to reduce the parasitic inductance, which is usually formed...
at the gate and also at source terminals in case of the SiC-MOSFET. RC snubbers and ferrite beads were proposed as solutions to overcome the side effects of these inductances in case of utilizing the SiC-JFET and the results showed the efficacy of these solutions. For further details, which are related to the effect of the RC snubbers and ferrite beads, see [35].

The efficiency improvement was not limited to the usage of the SiC-technology, but it was also possible to be achieved by the Si-technology by applying the soft switching techniques as in [36]. The resulted problems from the aforementioned method were the requirements of passive elements and in some cases to the auxiliary switches which will lead to increase the size and the cost of the inverter and in some cases the losses as well. Therefore, the optimized three-phase inverter design is still a challenging topic, especially in terms of obtaining a system with high efficiency, better thermal performance, minimum size and with enhanced EMI behavior. This behavior must comply with the standards that have been issued from the EMC organizations.

The consideration of the previous factors during the inverter design can be defined as the optimization requirements of the power inverter. The optimization of the voltage source inverters based on the SiC-technology is not covered until the present day; the reason behind this issue can be ascribed to the immaturity of the SiC-technology in power converters. On the other hand, many works in the literature were turning separately to the factors which affect the optimization in three-phase inverters, which were depending on Si-power switches. The main parameters which affect the inverter design have been reported in the literature and they have been summarized in a block diagram as shown in Figure 1.5.

The aforementioned block diagram will be used throughout this dissertation as a guideline during the inverter design based on the SiC-MOSFET. Moreover, the EMI behavior of the three-phase inverter with SiC-MOSFET will be predicated without commercial tools, based on the physical layout of the power circuit.

The importance of this EMI prediction returns to the presence of several high-power circuits in the EV, which can generate high-levels of the EMI, especially with the increased number of electrically driven loads in modern vehicles. This implies that the electronic systems have to be packed together in the limited space, which will increase the risk for electromagnetic interference between the different systems and it can cause the system malfunction or even the failure of the
SiC-devices. One of the sources, which affects the EMI behavior in the power inverter, is the switching speed. At high switching speeds, the quality of the output waveforms will be enhanced, but this will increase the tendency of the switching waveforms to oscillate due to the increased slew rates and the parasitic parameter effect. Accordingly, it is important to ensure that the power inverter will not harm the other systems; this concept is identified as the Electromagnetic Compatibility (EMC).

EMC implies that different electrical systems should be able to work in close proximity without affecting each other. From the EMC point of view, integration of electric traction drives in present vehicles represents a considerable challenge [37]. Therefore, all design parameters will be considered in this dissertation in order to fulfill the optimization requirements of the three-phase voltage source inverter based on the SiC-devices.

Figure 1.5: The main design parameters of power inverters.
1. 4. Main Objectives and Contributions

The main objectives and contributions of the presented work in this dissertation are:

- Examining electrical characteristics and the channel mobility behavior with temperature variations of the SiC-MOSFET.
- Designing a gate driver that meets the driving requirements of the SiC-MOSFET with better switching performance and with reduced EMI.
- Designing a new simplified control topology that leads to reduce the odd harmonics and to enhance the DC-link utilization in a three-phase inverter.
- Proposing a new method to compensate the dead-time in carrier-based PWM techniques.
- Designing and optimizing a 16 kW three-phase inverter with very high-efficiency and based on SiC-MOSFET, which is dedicated to EV applications.
- Modeling a three-phase inverter based on the physical layouts and analyzing the parasitic parameters and to compare the simulations with the empirical results in order to validate the theory.
- Designing faults detection and protection circuits that deal with overvoltage, overcurrent, short-circuit and overtemperature faults.

1. 5. Outline of the Dissertation

The work presented in this dissertation is divided into the following chapters:

**Chapter 2** provides a study of the effective channel mobility behavior in the SiC MOSFET with the temperature variations. The study will depend on the empirical electrical characteristics of the SiC MOSFET in order to extract the targeted behavior.

**Chapter 3** introduces a gate driver design which fits with the driving requirements of the SiC MOSFET. The effective parameters which affect the gate driver design have been studied and
their impacts on the driving losses have been presented, in addition to the relation between the switching behavior and the EMI behavior.

**Chapter 4** presents a three-phase voltage source inverter design with a rated power of 16 kW. The design aims at obtaining a high-efficiency system based on the usage of the SiC MOSFET as the main switching component. The design will lead to minimize the size of the cooling system for the aforementioned rated power, in addition to predict the EMI behavior of the inverter based on the physical construction of the power PCB in order to give designers the chance to check the compliance of their designs with the EMI standards before the production phase, which will save cost and effort.

**Chapter 5** proposes a new simplified method which represents the SVPWM by generating a modified reference signal to simplify the modulation process to become as simple as the traditional SPWM. The proposed method will retrieve the switching patterns of the SVPWM. The proposed method in this chapter is characterized by its simplicity of implementation and the reduction of the output harmonics in the output phase voltages and currents in contrast to other control topologies. Moreover, a new strategy for compensating the dead-time effect will be introduced as well.

**Chapter 6** presents four designed circuits to diagnose the common faults in the three-phase inverters and to protect the SiC-MOSFET and the driven load from the damage during the operation. The intended circuits which have been presented throughout this chapter are the overcurrent, short-circuit, overvoltage and overtemperature circuits.

**Chapter 7** presents an evaluation of the complete system in terms of the parameters that influence the efficiency of the three-phase inverters and the EMI behavior. This task can be performed by analyzing the contributions of inverter portions. In addition, the compliance of the power inverter to the EMC standards will be investigated in this chapter.

**Chapter 8** summarizes the outcomes of the dissertation and it shows the gained benefits and the outlooks of the study.
1.6. List of Publications


2. The Channel Mobility Behavior in SiC MOSFET with Temperature Variation

2.1. Introduction

The effective channel mobility is a key parameter that represents the capability of the power MOSFET to drive the current in addition to its ability to work as a reference that describes the velocity of the majority carriers [38]. The accuracy of the channel mobility measurements is a challenging issue in the Si and SiC–MOSFET, this is ascribed to the tremendous error sources, which might occur during the measurements, such as the gate leakage current and the series resistance. In this chapter, the behavior of the channel mobility as a function of the temperature is reported for the SiC-MOSFET. The determination of the effective channel mobility of the SiC-MOSFET will be obtained based on measuring of the electrical characteristics of the SiC-MOSFET and mainly the transconductance ($g_m$) will be employed to fulfill this task. The determination process will be achieved without prior knowledge of the physical dimensions of the channels of the investigated devices. Furthermore, the mobility reduction factor and the low field mobility behavior will be obtained at different junction temperatures.
2.2. On-State Resistance Behavior with Temperature Variation in SiC MOSFET

The examined SiC devices in this study are two SiC-MOSFETs from different manufacturers. The first one is SCT2080KE, which is manufactured by ROHM and it has identical ratings to the SCH2080KE SiC-MOSFET; the only difference between the two devices is the absence of the SBD in the SCT2080KE. The second device under investigation is C2M0080120D, which is manufactured by CREE and it has approximate rating levels to the ROHM’s counterpart.

Figure 2.1: The forward characteristics of C2M0080120D at different gate voltage levels (a) at 25°C (c) at 150°C; and The forward characteristics of SCT2080KE (b) at 25°C (d) at 150°C.
On-State Resistance Behavior with Temperature Variation in SiC MOSFET

The on-state resistance is one of the key features in the SiC-MOSFET due to its impact on the device losses and mainly the conduction losses, which represent the dominant portion of the device losses during the device operation. The on-state resistance of the SiC-MOSFET can be collected from the forward characteristics as shown in Figure 2.1 at 25 °C and at 150 °C, which represent the connection between the voltage drop over the SiC-MOSFET and the flowing current at different gate voltage levels; the slope of the drain current versus voltage drop in the quasi-saturation (ohmic region) and at a specific gate voltage represents the value of the on-state resistance.

The total on-state resistance in SiC MOSFETs consists of the group of resistances which represents the path of the current in the device during the conduction-state, which can be given by (2.1) as in [39] and they are depicted in Figure 2.2.

\[ R_{on} = R_{s}^* + R_{n^+} + R_{ch} + R_{a} + R_{epi} + R_{sub} \]  

(2.1)

Where:

- \( R_{s}^* \) : package resistance
- \( R_{n^+} \) : source layer resistance
- \( R_{ch} \) : channel resistance
- \( R_{a} \) : accumulation layer resistance
- \( R_{epi} \) : n-layer resistance
- \( R_{sub} \) : substrate resistance

The contribution of these resistances in the total on-state resistance SiC-MOSFET is altered by several design parameters, such as the blocking voltage. The channel resistance represents an important part in the on-state resistance and it determines the current conduction capabilities in the power semiconductor devices due to its relation with the channel mobility.

The channel contribution in the on-state resistance decreases with increased blocking voltage as reported in [40]. On the other hand, several works claimed the dominant contribution of the channel resistance in the total on-state resistance of the SiC MOSFET as in [2] and [6]. In [41], the negative temperature behavior of the on-state resistance with elevated temperatures up to 100 °C was claimed, which was returned to the larger reduction of the channel resistance in contrast to the increment of the other resistances (the drift and the JFET regions) within the prior temperature range. Beyond the 100 °C, the positive temperature behavior of the on-state
resistance was claimed, which will result in increasing the on-state resistance proportionally with the temperature.

Indeed, the previous behavior does not represent the real behavior of the on-state resistance in the SiC MOSFET and to show the real behavior, the on-state resistance with temperatures from 25 °C and up to 150 °C has been investigated. The devices under test were two SiC MOSFETs (SCT2080KE and C2M0080120D) and their results showed the positive temperature behavior of the on-state resistance for the entire temperature range (25 °C to 150 °C) as depicted in Figure 2.3.
2.3. The Relationship of the Channel Mobility and Transconductance

In this section, the relation between the channel mobility and the transconductance in the pinch-off region will be addressed. The aim is to exploit this relationship in order to extract the behavior of the channel mobility in the SiC-MOSFET with temperature variation. In the ohmic region, the channel resistance of the SiC MOSFET can be given by (2.2) as in [39]. It is important to notice the inverse proportional relationship between the effective channel mobility and the channel resistance. In this region, the drain current increases proportionally with the drain voltage and the MOSFET behaves like a resistor. Moreover, the drain voltage $V_D$ is less than $V_{GS}-V_t$ and the channel resistance can be given by (2.2).

$$R_{ch} = \frac{L_{ch}}{C_{ox} \cdot W_{ch} \cdot \mu_{eff} \cdot (V_{GS} - V_t)} \quad (2.2)$$

Where $L_{ch}$ represents the radial channel length, $W_{ch}$ is the entire channel width, $C_{ox}$ is the oxide capacitance per unit area, $\mu_{eff}$ is the effective channel mobility, $V_{GS}$ is the applied gate voltage and the $V_t$ is the charge threshold voltage. In the pinch-off region where ($V_D > V_{GS} - V_t$), the drain current remains approximately constant with increased drain-source voltage $V_{DS}$ and the equation (2.2) cannot be proven any more.

For the sake of finding the channel mobility, the extracted transconductance from the transfer characteristics can be employed. The transconductance of the SiC-MOSFET in the pinch-off region can be given by (2.3) as in [39].

$$g_m = \frac{W_{ch} \cdot \mu_{eff} \cdot C_{ox}}{L_{ch}} \cdot (V_{GS} - V_t) \quad (2.3)$$

Consequently, the mathematical formula of the effective channel mobility can be derived from the equation (2.3) and it can be represented as a function of the transconductance as in [39] and [42].

$$\mu_{eff} = \frac{L_{ch} \cdot g_m}{C_{ox} \cdot W_{ch} \cdot (V_{GS} - V_t)} \quad (2.4)$$
In order to investigate the channel mobility behavior with the temperature, the equation (2.4) can be modified by substituting the parameters which have temperature dependency, as functions of temperature. Hence, the channel mobility with temperature variation can be given by equation (2.5).

\[
\mu_{\text{eff}}(T) = \frac{L_{\text{ch}} \cdot g_m(T)}{C_{\text{ox}} \cdot W_{\text{ch}} \cdot (V_{\text{GS}} - V_t(T))}
\]  

(2.5)

At first, it is necessary to find the transconductance \( g_m \) of the investigated devices at different temperatures; this can be fulfilled by investigating the transfer characteristics at specific \( V_{\text{DS}} \). In this work, the transfer characteristics have been collected at \( V_{\text{DS}}=10\,\text{V} \) as shown in Figure 2.4 and based on equation (2.6).

\[
g_m = \frac{\delta I_d}{\delta V_{\text{GS}}} \text{ at } V_{\text{DS}} = \text{Constant}
\]  

(2.6)

The transconductance was collected within the linear region, which is given by the slope of the dotted line as depicted in Figure 2.4. It is important to avoid the transconductance measurements at low gate voltages, because they demonstrated negative temperature behaviors at these gate voltage levels.

The necessity to obtain accurate measurements returns to the dominant dependency of the channel mobility behavior on the transconductance and the threshold voltage measurements within the investigated temperature range. Figure 2.4 shows the transfer characteristics and the transconductance measurements of the investigated devices at 25 °C and at 150 °C. In addition, the complete transconductance behavior versus the temperature is depicted in Figure 2.5.
Moreover, the investigation of the electrical characteristics of the SiC-MOSFETs can lead to find other parameters, which are helpful in better understanding the behaviors of these devices; such as the low field mobility and the mobility reduction factor, which will be denoted by $\mu_o$ and $\theta$, respectively. The mobility reduction factor can be extracted using (2.7), as proposed in [43].

$$\theta = \frac{I_d}{(g_m \cdot (V_{GS} - V_t)) - 1}$$  \hspace{1cm} (2.7)$$

Typically, the channel mobility of the SiC-MOSFET suffers from the degradation by increasing the applied gate voltage and the amount of this reduction is defined by the channel mobility reduction factor and it is denoted by $\theta$ in (2.7) as in [43]. The relation between the channel mobility, the mobility reduction factor and the low field mobility can be summarized in equation (2.8).

$$\mu_{eff} = \frac{\mu_o}{1 + \theta \cdot (V_{GS} - V_t)}$$  \hspace{1cm} (2.8)$$
In order to find the threshold charge voltage, the $I_d/(g_m)^{0.5}$ curve was used as a function of $V_{GS}$ as proposed in [43]. Hence, the threshold voltage was extracted at the voltage point at which the investigated SiC-MOSFETs begin to conduct as shown in Figure 2.6 at 25 °C and 150 °C. Accordingly, the threshold voltage behavior of the devices under test with temperature variation is shown in Figure 2.7.

Furthermore, the maximum transconductance of the SiC-MOSFET can be found at the slope of $I_d/(g_m)^{0.5}$ versus $V_{gs}$ in the linear region as shown in Figure 2.7. The identification of the maximum transconductance based on the aforementioned method was reported in [43]. The extracted values are expected to be higher than the direct method, i.e. based on the transfer characteristic in the linear region, which will be dealt with later in this work.
The determination of the threshold voltage and ascertaining the transconductance $g_m$ of the investigated devices from their transfer characteristics can be exploited for the sake of evaluating the mobility reduction factor based on equation (2.7).

![Figure 2.6: Threshold voltage determination approach from $I_d/(g_m)^{0.5}$ vs gate voltage for SCT2080KE (left) and C2M0080120D (right) at 25 °C and 150 °C.](image)

![Figure 2.7: The determination method of maximum transconductance (left) and the threshold voltage behavior versus temperature of SCT2080KE and C2M0080120D (right).](image)
2.4. The Channel Mobility Behavior with Temperature Variation

In order to find the effective channel mobility of the SiC-MOSFET based on equation (2.5), it is necessary to have prior knowledge of the channel length $L_{ch}$ and the channel width $W_{ch}$ as well as the gate oxide capacitance $C_{ox}$. Therefore, the channel length and the entire width of the channel in the investigated SiC-MOSFET were considered 1 $\mu$m and 400 m per cm², respectively. The area of the gate pad was considered 0.1 mm² in contrast to 0.4 mm² as reported in [44] for CPM2-1200-0080B, which has similar ratings to the investigated devices. The width of the channel here corresponds to the circumference of the single cell multiplied with the number of cells [39]. The oxide capacitance per unit area can be found by (2.9) assuming a thickness of 50 nm based on [39].

$$C_{ox} = \varepsilon_{ox}/t_{ox}$$  \hspace{1cm} (2.9)

Where $\varepsilon_{ox}$ represents the dielectric constant of the silicon dioxide and $t_{ox}$ represents the thickness of the gate oxide which is normally less than 100 nm. Therefore, the chosen thickness will result in approximately 70 nF/cm² as oxide capacitance $C_{ox}$ considering that the relative permittivity of the SiO₂ equals 3.9. According to the extracted data and the considered dimensions and based on equation (2.5), the effective mobility with temperature variations was evaluated for the investigated SiC MOSFETs. Figure 2.8 shows the aforementioned behavior versus the temperature of the two devices.

![Figure 2.8: Effective channel mobility versus the temperature of C2M0080120D (left) and the effective channel mobility versus the temperature of SCT2080KE (right).]
The results showed approximate levels of the channel mobility in case of SCT2080KE and the C2M0080120D, which was in the range of 14.5-17.5 cm².V⁻¹.s⁻¹ for SCT2080KE in contrast to 14.5-17.9 cm².V⁻¹.s⁻¹ for the C2M0080120D. Finally, both showed a decrement of the channel mobility with elevated temperatures. The previous results represent the channel mobility of the investigated SiC planar MOSFET in contrast to a measured channel mobility of 11 cm².V⁻¹.s⁻¹ for the double trench SiC MOSFET on the trench side walls as reported in [5].

In conclusion, the effective channel mobility in the investigated SiC MOSFETs showed an inverse proportional behavior at elevated temperatures, which confronts with the results in [45] and [46]. The reduction of the effective channel mobility corresponds to the increment of the on-state resistance due to the dominant increment on the (JFET and the drift regions) resistances which are characterized by a positive temperature dependency. At the end, this will lead to an increase in the total on-state resistance versus the temperatures as shown in Figure 2.3. These results disprove the claims in [41] and [46] about the negative temperature coefficient behavior of the on-state resistances in the SiC-MOSFET with elevated temperature lower than 100 ºC. In fact, the channel mobility behavior with temperature variation is dependent on the level of the background doping concentration as reported in [47], which explains the inconsistent claims of increasing or decreasing the channel mobility of the SiC MOSFET with temperature variation.
CHAPTER 3

3. Driving of SiC-MOSFET

3.1. Introduction

Recently, several works have been aiming at designing power applications based on the SiC devices as presented in the section of the state of art. On the other hand, both driver and signal conditioning issues are not addressed so frequently [27], [11]. At the time of writing this work, only very few works (as in [48]) have discussed the driving requirements of the SiC-MOSFET in comparison with the driving requirements of other SiC devices as in [49], but not limited to [50], [20]. Therefore, the proper design of the gate driver for the SiC-MOSFET will be discussed within this chapter by analyzing the effect of the design parameters on the switching behavior and the EMI behavior. The driving requirements of the Si-MOSFET and other Si-devices have been discussed in detail in the literature and this matured experience can be exploited and expanded to fit with the driving requirements of the SiC-MOSFET by considering the differences between the two technologies and by modifying the previous works. In fact, several approaches are possible to design the gate driver of the SiC-MOSFET; one of these approaches depends on modifying the former circuits of the Si-MOSFET and improving the features to pace with the SiC-MOSFET demands. Another possibility relies on starting the design from the scratch; in the end, both design approaches must be committed to the general design rules.
In this work, the first approach was chosen; therefore, the different types of the gate drivers for Si-MOSFET were studied and analyzed; further details about these types can be found in [51]. The previous study was trying to show the main differences between the driving requirements of the Si-MOSFET and the SiC-MOSFET, which can be summarized in the requirements for higher output voltage levels for the benefits of the SiC-MOSFET. In addition, the gate driver design has to propose solutions to overcome or at least to reduce the oscillation problem, which appears in the SiC-MOSFET behavior during the switching transition. Finally, one of the requirements of the gate driver of the SiC-MOSFET is the ability to provide faster switching speeds. The importance of this consideration appears clearly in several applications, such as the PV-inverter in which the switching speed is an important design parameter. In fact, the main source of the oscillations in the SiC-devices proceeds from the strong impact of the parasitic parameters which are forming due to the high frequency components in the switching waveforms and the inductive behavior of the traces at these frequencies.

### 3.2. Driving Requirements of SiC Devices

The first step in designing the gate driver is the determination of the targeted applications in order to consider the necessities of these applications. In this work, the designed gate driver has been dedicated to the Electrical Vehicles (EV) applications. Consequently, the proper design of the gate driver must include a full understanding of the characteristics of the driven device, which will be driven by the designed gate driver. The utilized device in this work was a 1.2 kV/35 A SiC-MOSFET, which is manufactured by ROHM Semiconductor.

The static characteristics of the investigated component have been extracted in order to find the optimal operating point which meets the minimum on-state resistance. Thus, a high-power curve tracer (Sony Tektronix, 371B) was used to extract the static characteristics of the SCH208KE as depicted in Figure 3.1. The on-state resistance $R_{ds(on)}$ was measured at $I_D=20$ A and $V_{GS}=20$ V and measurement showed that $R_{ds(on)}$ was 89 mΩ at $T_J=25$ °C and 113 mΩ at $T_J=150$ °C.

It is certain that the gate driver circuit is a vital part in any switching converter; in consequence, the proper selection of the gate driver components and the best layout will lead to a robust gate driver design in terms of the electromagnetic interference and the reduction of total losses of the driven device including switching losses and conduction losses.
In fact, characteristics of MOSFETs change according to three key parameters, which have been summarized in Table 3.1. These parameters influence the gate driver design and they represent; the positive gate voltage \((+V_{GGon})\), the negative bias gate voltage \((-V_{GGoff})\) and the external gate resistance \((R_g)\). Hence, it is important to set these parameters so that the SiC-MOSFET capabilities can be exploited.

The first parameter which to be set is the gate voltage, which must be set so that the SiC-MOSFET has the minimum conduction losses. Therefore, \(V_{GGon}\) was set to 20 V based on the static characteristics, which is located within the rated gate voltage \(V_{GS}\), \((V_{GSRated} = -6 \text{ V} \ldots 22 \text{ V})\). Furthermore, the selected gate voltage level should be higher than the temperature coefficient point \((TCP)\), which represents the marginal line between the thermal stability and thermal instability areas as displayed in Figure 3.1. This margin ensures that the device operates in the positive temperature coefficient area.

Correspondingly, it is recommended to use a negative gate bias voltage with SiC-MOSFETs during the turn-off in order to reduce the switching time; on the other hand, the driving losses then become higher. Therefore, \(V_{GGoff}\) was set to -0.7 V, which was sufficient to afford the demanded switching time (less than 100 ns). The second step toward the design should be the evaluation of the gate driving losses by investigating the dissipated power, which can be expressed by [52]:

\[
P_{\text{gate}} = (V_{GGon} + |V_{GGoff}|) \cdot Q_{\text{gate}} \cdot f_{\text{sw}}
\]  

\((3.1)\)

Where \(Q_{\text{gate}}\) represents the maximum gate charge value which has been extracted from the switching characteristics of the SiC-MOSFET with the measured value at approximately 100 nC, whereas \(f_{\text{sw}}\) represents the switching frequency set to 20 kHz; this resulted in a 50 mW as the dissipated power in the gate driver.
Figure 3.1: Output characteristics of the SCH2080KE MOSFET at 25 ºC (left); the transfer characteristics at $V_{DS}=10V$ and thermal stability (right).

The second parameter which affects the switching time and switching losses is the external gate resistance, where the lower gate resistance means faster switching speed and lower driving losses. On the other hand, this will result in increasing the electromagnetic interference (EMI) owing to the surge voltage during switching, which becomes larger. A tradeoff between the switching losses and the EMI should be considered. Therefore, the selected values of $R_G$ which will be under investigation are 5 and 10 Ω. Now, the drive current peak value $I_{gp}$ can be calculated as in [52].

$$I_{gp} = \frac{V_{GGM} + |V_{Goff}|}{R_G + R_g}$$

(3.2)

Where $R_G$ is an external gate resistance and $R_g$ is the internal MOSFET gate resistance. Therefore, $I_{gp}$ should be 1.3 A in case of 10 Ω gate resistance. The average value of the driver current using the gate charge characteristics can be given by the equation (3.3) as in [52]

$$+I_g = -I_g = f_{sw} \cdot (Q_g + C_{iss} \cdot |V_{GS}|)$$

(3.3)

Where, $C_{iss}$ is the input capacitance of the SiC - MOSFET.
### 3.3. Low-Side Driver Design

Considering the parameters which are listed in Table 3.1; a low side gate driver has been designed as presented in Figure 3.2. The circuit consists of three main parts; the control signals and the optocouplers, which ensure the isolation between the control circuit and the power circuit. The second part represents the LTC4444 driver IC which is manufactured by Linear Technology and it is capable of generating complementary pulses with a maximum output voltage equal to 13 V. The final part in the proposed circuit consists of two n-channel MOSFETs with model number PSMN2R8-25MLC, which are made by NXP Semiconductors and which are represented in Figure 3.2 by T₁ and T₂.

| Main Characteristics | (+V\text{\textsubscript{G\text{\textsubscript{on}}}}) rise | -|V\text{\textsubscript{G\text{\textsubscript{off}}}}| rise | (R\text{\textsubscript{g}}) rise |
|----------------------|---------------------|---------------------|---------------------|
| \(R_{\text{ds(on)}}\) , \(V_{\text{DS(sat)}}\) | Fall | - | - |
| \(t_{\text{on}}, E_{\text{on}}\), Short-circuit withstand capability | Fall | - | Rise |
| \(t_{\text{off}}, E_{\text{off}}\) | - | Fall | Rise |
| Peak current (during transistor On-state ) | Rise | - | Fall |
| Peak voltage (during transistor Off-state ) | - | Rise | Fall |
| \(\text{di/dt, dv/dt}\) | Rise | Rise | Fall |

Table 3.1: SiC-MOSFET driving conditions and main characteristics

The previous transistors have been chosen due to their low parasitic inductance and the ultra-low gate charge, being designed for high system efficiency. Aforementioned features will lead to very fast switching capabilities and will provide the required voltage level to the output of the gate driver. The performance of the proposed design has been compared to the gate driver with product number of FOD3180 from Fairchild in order to investigate the validity of the proposed design. The proposed driver can provide a positive voltage level up to 25 V and down to -6 V as the negative bias voltage at driver output. The maximum switching frequency was investigated up to 500 kHz. The output pulses of the gate driver up to 200 kHz showed no change in the waveforms features, but when the switching frequency reaches 500 kHz the output pulses will suffer from distortions in the duty cycles and in their features. The impact of the switching speed on the driver’s output is depicted in Figure 3.3. The proposed design showed superiority in comparison with the available drivers.
The proposed design could provide pulses at the driver’s output with a rise time between 30ns and 75 ns; and 30 ns up to 70 ns in the case of the fall time within the tested switching frequency range. The proposed driver has been set to provide 20 V at the output and -0.7 V as a negative voltage level during the switching off. While the FOD3180 gate driver was investigated within the same switching frequency range, the rise and fall time were approximately 30 ns. The proposed gate driver showed higher ripples in the output voltage pulses due to the impact of stray inductances of the PCB traces. These ripples can be reduced by using a small filtering capacitor of 0.1 µF in parallel to the power sources of the gate driver. The effect of the filter capacitor of 0.1 µF in reducing the output ripples is depicted in Figure 3.4.

This problem does not exist in the case of the FOD3180, because it is compact in an IC package. Briefly, the proposed design could provide a better rise time and fall time leading to an enhancement of the switching behavior and the EMI behavior as will be shown in the following sections, in addition to its flexibility to provide a positive and negative voltage level at the output, which will cover the whole rated range of the gate voltage of the SiC-MOSFET. The reference driver in the investigated comparison is FOD3180, which is manufactured by Fairchild and it is rated to provide 20 V as a maximum output voltage level and 0 V. Since the fast switching and
the low oscillations are considered as design requirements in the proposed design, the effect of the stray inductance in the driver circuit must be minimized. This reduction was fulfilled by placing the gate drivers to the SiC-MOSFET as close as possible, which is considered during the PCB layout.

![Graphs showing output voltage vs time for proposed and FOD3180 driver at different frequencies](image)

Figure 3.3: Gate drivers output of proposed (red) and FOD3180 (green) at different frequencies: 20 kHz (first row) and 500 kHz (second row).

The results exhibited a reduction in the peak voltage and current oscillations during the turn-off by the proposed driver in contrast to FOD3180 due to the slower slew rate of the drain current, which will lead to a reduction of the effect of common gate-source coupling.
3.4. Evaluation of the Gate Drivers of the SiC-MOSFET's

For the sake of investigating the proposed design; an inductive load double pulse tester was used to analyze the switching behavior of the SCH2080KE SiC-MOSFET using the proposed driver and the FOD3180 driver. The input voltage of the double pulse test was set to 800 V; a 1800 V DC capacitor with 420 µF capacitance made by WIMA was used as a DC-Link capacitor and 1200µH inductor in parallel with a 1.2 kV/20 A SiC Schottky barrier diode. Figure 3.5 depicts the switching characteristics of the SCH2080KE SiC-MOSFET using the two drivers during the turn-on and turn-off. The rest of the oscillations resulted from the parasitic elements which consist of the parasitic capacitances resulting from the turns of the loading inductor $L_1$ and the junction of the diode $D_1$ and it is characterized in Figure 3.2 by $C_t$. In addition, the parasitic inductance which is denoted in Figure 3.2 by $L_d$, which occurs between the loading inductor and the drain of SiC-MOSFET, has a part in these oscillations.

The last parameter which engages in the generation of the oscillation during the turn-off transition is the output capacitance of the SiC-MOSFET ($C_{oss}$). Regarding the overshoot current, the proposed design revealed to approximate overshoot current and lower oscillations during the turn-on in contrast to FOD3180, despite of incrementing the slew rate of the drain current which

![Figure 3.4: The output signal of the proposed gate driver without filter capacitor (left) and with filter capacitor of 0.1µs (right).](image-url)
was eight times higher. This increment will lead to reduce the switching losses and it will enhance the performance from the EMC perspective.

![Figure 3.5](image)

Figure 3.5: Switching characteristics using FOD3180 gate driver; turn-on characteristics (top right) and turn-off characteristics (top left). Switching characteristics using the proposed driver; turn-on characteristics (bottom right) and turn-off characteristics (bottom left). All measurement collected at room temperature and $R_G=10\Omega$.

The overshoot current during the turn-on resulted as an aftereffect of the parasitic capacitance $C_t$, which will behave as a resonance circuit with the loading inductor $L_1$. The parasitic inductance $L_s$ has a big influence on the switching behavior in terms of producing overshoot current during the turn-on transition and it slows down the transition during the turn-off. Moreover, this parasitic will couple with the gate driver circuit due to the common ground and therefore, its effect must be...
minimized. The minimization of the gate-source inductance can be realized by placing the gate driver to the SiC-MOSFET as close as possible and also by choosing the proper gate resistor value, which will result in damping of the oscillations as will be discussed in the coming subsections.

The empirical results showed an 872 µJ as lost energy during the turn-on transition in the proposed driver versus 2200 µJ in FOD3180. Thus, the turn-off energy losses have been measured and the lost energy during the turn-off revealed 168 µJ in the designed driver in contrast to 281 µJ in FOD3180. These improvements will induce a reduction in the switching losses as a result of using the proposed driver up to 60% lower than the FOD3180 losses.

Moreover, the proposed driver showed lower oscillations during the switching transition. This will lead to reduce the EMI, which are formed as a result to the oscillations with a time period of less than 10ns. It is worth mentioning that the resulted losses in these measurements were higher than the values which have been extracted from the datasheet and which have been summarized in table 1.1. This returns to the higher values of the used gate resistor and the loading inductor; these values were 10 Ω and 1200 µH in contrast to 0 Ω and 500 µH as mentioned in the datasheet. Both of them will slow down the switching transition and increase the losses.

### 3.4.1 Parameter Effects on Switching and EMI Behavior

In this part, the effects of the main parameters which influence the switching characteristics and the EMI behavior will be analyzed by studying the influences of the gate resistors, the applied gate voltage and the switching frequency. Therefore, three levels of gate voltage with values 15 V, 18 V, 20 V have been applied to the gate of the SiC-MOSFET. The results show no impact of the applied gate voltage on the switching behavior except during turn-on voltage, where a higher gate voltage resulted in reducing the rise time, which will lead to an increase in the switching speed; on the other side, it will induce a higher EMI.

Moreover, the influence of two different external gate resistors with values of 5 Ω and 10 Ω have been investigated and the outcomes showed that the gate resistor value has the dominant impact on the switching characteristics and the EMI behavior as shown in Figure 3.5 and Figure
3.6, respectively. The utilization of a higher gate resistance resulted in speeding up the slew rate of the voltage drop behavior during turn-off transition; this might also increase the overshoot voltage due to the increment of the transition slope and the effect of the parasitic inductance ($L_d$), which is shown in Figure 3.2. On the other hand, $R_G$ with 5 Ω value caused a higher ringing current during the turn-on transition of the SiC-MOSFET than $R_G$ with 10 Ω, which will cause a radiated EMI as a result of the small oscillations with widths of less than 10 ns. On the contrary, the higher gate resistor during the turn-off was leading to slow down the transition of the output voltage $V_{DS}$ during the turn-on.

One of the proposed solutions to deal with this issue is to use different gate resistors during the on and off states, which will result in reducing the rise and fall time. It is possible to obtain a transition time close to 10 ns which will lead to mitigate the effect of the parasitic parameters. A voltage dive was formed during the turn-on voltage transition in case of $R_G$ with 10 Ω as shown in Figure 3.5 due to the voltage drop over the parasitic inductance.

In order to choose the legitimate gate driver; the designer should compromise between switching speed and EMI based on the design requirements and priorities. This work is even going further by analyzing the influence of the design parameters on the EMI behavior. The effect of changing gate voltage levels, gate resistor values and switching frequencies can be investigated by analyzing the effects of these parameters within the conducted and radiated EMI range. The conducted EMI range is defined in the EMC regulations to cover a 450 kHz to 30 MHz range. The conducted EMI measures the amount of EMI that can be conducted by the gate driver, whereas the radiated EMI covers 30 MHz to 1 GHz and it represents the amount of EMI which is radiated by the gate driver circuit.
Evaluation of the Gate Drivers of the SiC-MOSFET's

Figure 3.5: The effect of the gate resistors on turn-off voltage (top left); on the turn-on current (top right); on the turn-on voltage (bottom right). The effect of gate voltage on the turn-on voltage at $R_G=5\ \Omega$ (bottom left).

The two types of EMI have been investigated by analyzing the FFT of the extracted experimental gate voltages, which have been uploaded to LTspice IV software to use the software FFT tool. Figure 3.6 shows the conducted and radiated EMI spectrums in different cases. The first case includes different gate voltages. The EMI spectrum shows a small impact of the gate voltage levels on the conducted EMI, while the EMI reduction was in the order 1 to 3 dB. On the contrary, the reduction of the gate voltage level produced EMI peaks in the radiated EMI range.
Evaluation of the Gate Drivers of the SiC-MOSFET's

Figure 3.6: EMI spectrum including conducted and radiated bands in case of different switching frequencies (top left); different gate resistors (5 Ω and 10 Ω) (top right); different gate voltages (bottom left) and EMI spectrum of the proposed circuit and FOD3180 (bottom right).

Finally, the effect of increasing the applied gate resistor shows no impact on the conducted EMI up to 1MHz, but it causes a reduction in the order of 60 dB in the radiated EMI. The switching frequency reveals no influence by changing the gate resistor in the radiated range as shown in Figure 3.6, but it leads to an increment in the conducted EMI, owing to the reduction of the rise and fall time.

Thus, an increment takes place in the current and voltage change rates which are the main reasons of the EMI. Finally, the proposed design has been validated by comparing the EMI behavior of the proposed circuit with the FOD3180 gate driver at the same gate voltage and gate resistor; the results presented a reduction in the conducted EMI of more than 5 dB and little enhancement within the radiated EMI range.
3.5. High Side Driver Circuit

The selection of the suitable method to power the insulated side of the high side driver is considered as a controversial topic, due to the variety of the implementation possibilities, which aim at providing the high side drivers with a distinctive level of insulation. These approaches might use the gate driver transformer, passing through the dedicated power supplies and half bridge bootstrap configuration, ending with integrated power circuits [53]. Each of the previous methods has its advantages and disadvantages, which makes the final choice in the hand of the designer even more difficult meeting the design requirements.

The usage of the transformer in insulating the high-side gate driver shows simplicity in operation and limited requirements in terms of the components number, but on the other hand, the transformer gate drivers suffered from problems in the duty cycle and core saturation, which usually result from the fast change in the duty cycles. In addition, the transformer gate driver has a drawback related to the high cost of the transformers. The second option is the usage of the dedicated power supplies, which has no limitation on the duty cycle and it permits more degree of freedom in controlling the input pulses, but it has the time shift problem as a drawback and it is also inconvenient and expensive in EV applications. Indeed, the selection of the insulation strategy is totally related to the design requirements and applications, which can be considered as the case of SiC-MOSFET not trivial to be met.

Recently, several works have been discussing the benefits of utilizing the DC-DC converter in order to provide the optimum power rails for driving IGBTs as in [52], [54] and [55]. The SiC-MOSFET requirements can be summarized in providing the suitable gate voltage swing with an insulation and immunity to the noise capabilities in order to enhance the switching behavior and to reduce the driven devices losses. Furthermore, it should comply with the EMC requirements for the applications. Therefore, two levels of DC-DC choppers are used in the proposed design to meet the previous requirements for powering the driver of SiC devices.

The proposed circuit as demonstrated in Figure 3.7 consists of four levels; the first level contains a +5 V supply followed by a low-pass filter to minimize the noise and the ripples of the supply. The second level is a step up DC-DC converter, which has the model number JCB0305S24-3W to step up the voltage level from +5 V to +24 V. The third level is represented by a DC-DC step-
down converter with the model number MP1584-3A which will be used to regulate the output voltage to the required voltage level (+20 V) to supply the driver of the SiC-MOSFET. The idea behind using two levels of DC-DC chopper is the lack of DC-choppers which afford an output voltage of 20 V.

Figure 3.7: Insulated gate driver powered from DC-DC choppers.

The required output voltage can be set by changing the values of the resistors $R_{16}$, $R_{17}$, $R_{18}$ and $R_{47}$, which will be used to control the output of the step-down converter. The relation of the values of the resistor and the output voltage can be found in the product datasheet. The output voltage of the previous stages is set to +20 V in order to feed the drivers with the required voltage level and also to provide the insulation for the high side driver. The control pulses of the gate driver were applied independently in the proposed design, which will provide insulation and protection capabilities of the controller due to their ability to withstand 5000 V (rms) for one minute. The rise time and fall time of the FOD3180 gate driver was investigated for a switching frequency range of 5 kHz up to 500 kHz and the gate driver showed a good performance. Figure 3.8 shows the output of the FOD 3180 gate driver at 50 kHz.
The next step is to investigate the previous settings by a double pulse tester circuit, using the same configuration of the low side driver, but with exchanging the position of the device under test (DUT) from the bottom side to the top side; the same applies to the diode and the parallel coil. The experimental outcomes confirm the validity of the design with the same range of the rise time and fall time during the turn-on and turn-off. In addition, the usage of the separated drivers for the top and bottom side can lead to some delay between the output voltages; this delay has been measured and it was negligible; reaching approximately 25ns as shown in Figure 3.9.

Figure 3.9: The synchronization between the output voltages of the high and the low side drivers.
4. Three-Phase Voltage Source Inverter Using SiC-MOSFETs - Design and Optimization

Recent research has highlighted the benefits of SiC devices as an alternative to the Si-devices in various applications as reported in [23], [56] and [57] owing to the superior characteristics of the SiC-technology as in [58] and [59]. The three-phase inverter is considered as one of the beneficiaries from this technology due to the expectation of obtaining new and higher efficiency levels that are impossible to achieve by the current Si-devices [26] without much effort. Hence, it is also expected from this technology to reduce the cooling system size and cost. In this chapter, a three-phase voltage source inverter prototype with high efficiency and with a rated power of 16 kW will be implemented. The switching and conduction losses of the SiC-MOSFETs will be analyzed to show their benefits in VSI application.

The optimal operating point of the power inverter will be preset. The design is even going further by analyzing the stationary thermal model of the inverter and it shows roughly the procedures for selecting the proper heat-sink, which minimizes the cooling size and cost. Moreover, EMI parasitic parameters will be extracted for the Voltage Source Inverter (VSI) in terms of the power circuit layout and the heat-sink effect. The analysis aims at showing the possibility of calculating these parameters without the use of commercial software tools. Finally, the previous steps will
lead to an optimized three-phase VSI design. The work will continue with a comparison between the predicted and experimental results in order to verify the proposed prediction model within the conducted EMI range.

### 4.1. Three-Phase Inverter Design

The first step in the proposed design is to study the characteristics of the power switches which will be used in the power circuit of the VSI. The used power switch was SCH2080KE SiC-MOSFET 1.2 kV/40 A, manufactured by ROHM Semiconductor and it was chosen due to its ability to work with the required design specifications which have been summarized in Table 4.1 and due to its special characteristics in terms of the total losses in case of driving the SiC-MOSFET properly as explained in Chapter 3.

The static and dynamic characteristics of the selected SiC-MOSFET have been investigated in order to find the optimal operating point which will result in minimizing the power losses in the VSI during the operation at different temperatures. In addition, an overview of the losses in the VSI has been compiled to confirm the SiC device operation within the safe operating area. Figure 4.1 shows the forward characteristics of the SCH2080KE SiC-MOSFET at temperatures 25 °C and 150 °C, respectively. The operating point was located at an effective on-state drain current equal to 10 A, which results in a voltage drop equal to 1.5 V at 25 °C and 2.2 V at 150 °C in case of applying 20 V as gate voltage. The gate driver circuits have been created to meet the required operating point and the complete design was discussed in [60] and in Chapter 3.

<table>
<thead>
<tr>
<th>DC-link voltage, ( V_{dc} )</th>
<th>800V</th>
<th>Switching frequency ( f_{sw} )</th>
<th>( f_{sw}=5\text{kHz} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line to line voltage</td>
<td>( V_{LL,\text{rms}}=\frac{1}{\sqrt3}V_{dc}=462\text{V} )</td>
<td>Fundamental frequency</td>
<td>( f_o=50\text{Hz} )</td>
</tr>
<tr>
<td>Effective phase voltage</td>
<td>( V_{ph,\text{rms}}=V_{dc}/3 \approx 267\text{V} ) (SPWM)</td>
<td>Power factor = ( \cos\theta )</td>
<td>( P_F=0.9 ) lagging</td>
</tr>
<tr>
<td></td>
<td>( V_{ph,\text{rms}}=V_{dc}/\sqrt8 \approx 283\text{V} ) (CB-SPWM)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output power</td>
<td>( P_o=3\cdot V_{ph,\text{rms}} \cdot I_{\text{rms}} \cdot \cos\theta = 16.2\text{kW} )</td>
<td>Modulation Index</td>
<td>( M=1 )</td>
</tr>
</tbody>
</table>

**Table 4.1: The Inverter Design Specifications**

Proceeding from the aforementioned points, the conduction and the switching losses are measured in case of sinusoidal PWM with modulation index equal to 1. The effective output current in the designed voltage source inverter has been set at \( I_o(\text{rms}) = 22.5 \text{A} \), based on the
previous operating point. Hence, the peak output current was \( I_{o(peak)} = I_o = 31.8 \) A. Thus, the conduction loss of each MOSFET can be given by (4.1) as in [61]. As a result, the total conduction losses of the six MOSFETs in the inverter can reach up to 108 W at an effective drain current of 15 A and at room temperature. The SiC MOSFET is a semiconductor device which has a positive temperature coefficient, which means that conduction losses will become higher with increased temperatures. Therefore, the conduction losses of the six MOSFETs will reach up to 128.5 W at 80 °C and 153 W at 150 °C. For the sake of finding the conduction losses of each SiC MOSFET in the power inverter, equation (4.1) can be used.

\[
P_{CM} = I_{on(rms)}^2 \cdot r_{ds(on)} = I_o^2 \cdot r_{ds(on)} \cdot \left( \frac{1}{8} + \frac{M \cdot \cos \theta}{3\pi} \right) \tag{4.1}
\]

The conduction losses of the SiC-MOSFET represent the dominant losses in the three-phase inverter in contrast to the other SiC devices, such as SiC BJT. On the other hand, the SiC-MOSFET demonstrates lower switching losses than its counterparts at the same switching speed, due to the low input capacitances, which are considered to be a main reason of its ability to switch faster than other SiC devices. Equivalently, the switching losses have to be taken into account during the design phase in order to find the total consumed losses of the inverter.

The previous step is necessary for the heat-sink selection as well as for the optimization of the inverter design in terms of the EMI behavior by choosing the proper switching parameters during the transition. This will result in the minimization of the switching losses and also in the reduction of EMI. The task can be accomplished by a compromise between the switching speed and the slew rate of the drain current and the voltage drop on the SiC-MOSFET during the switching transition.

The worst-case turn-on energy losses in each power MOSFET \((E_{onM})\) can be calculated as the sum of the turn-on energy, without taking the reverse recovery process into account and it is denoted by \((E_{onM})\) and the turn-on energy, which is caused by the reverse-recovery of the integrated Schottky diode denoted by \((E_{onMrr})\) and they can be expressed by (4.2) and (4.3) as in [61].
The turn-on and turn-off switching energies are calculated based on the equations (4.2) and (4.3) respectively. They have been compared with the values, which have been extracted from the double-pulse test. The following data has been extracted from the SCH2080KE datasheet, where the rise time of the drain current during the turn-on transition was $t_{ri}=34 \text{ ns}$.

The falling time of the voltage drop was $t_{fu}=44 \text{ ns}$, the reverse recovery charge was $Q_{rr}=60 \text{ nC}$, the applied input DC voltage was $V_{dc}=800 \text{ V}$, the rising time of the voltage drop during the turn-off transition was $t_{ru}=30 \text{ ns}$, the falling time of the drain current during the turn-off was $t_{fi}=50 \text{ ns}$ and $I_{on(rms)}=10 \text{ A}$. Therefore, the turn-on switching energy was $331 \mu\text{W}\cdot\text{s}$; similarly, the turn-off energy was found to be $560 \mu\text{W}\cdot\text{s}$.

The measured turn-on energy and the turn-off energy of the FOD3180 driver were $687 \mu\text{W}\cdot\text{s}$, $181 \mu\text{W}\cdot\text{s}$, respectively. Likewise, the utilization of the gate driver which was presented in Chapter 3 and which was proposed in [60], can reduce the switching losses. The last driver offers $253 \mu\text{W}\cdot\text{s}$ as turn-on energy and $274 \mu\text{W}\cdot\text{s}$ as turn-off energy as shown in Figure 4.2, which means a $39\%$ reduction of the switching losses. The previous measurements have been collected at identical DC input voltages and equivalent operating points. According to the measured values, the switching losses have been calculated based on (4.4) and similarly as in

![Figure 4.1: Forward characteristics of SiC-MOSFET (SCH2080KE) at 25 °C (left) and at 150 °C including the resistance of the measurement cables of $110 \text{ m}\Omega$ (right)]
at a switching frequency of 5 kHz, so the total switching losses of the six MOSFETs were 26 W by using FOD3180 gate driver and 15.8 W by the proposed gate driver in this work.

\[ P_{\text{sw,M}} = (E_{\text{on,M}} + E_{\text{off,M}}) \cdot f_{\text{sw}} \]  

(4.4)

The SCH2080KE SiC-MOSFET contains an internal parallel Schottky diode with a measured on-state zero current voltage \( V_{d0} = 0.7 \) V, the on-state diode resistance is \( R_d = 30 \) m\( \Omega \). By assuming sinusoidal PWM, the conduction loss of the Schottky diode has been measured and compared to the calculated value. Consequently, the conduction losses can be given by (4.5) as in [61].

\[ P_{\text{CD}} = V_{d0} \cdot I_o \cdot \left( \frac{1}{2\pi} - \frac{M \cdot \cos \delta}{8} \right) + R_d \cdot I_o^2 \cdot \left( \frac{1}{8} - \frac{M \cdot \cos \delta}{3\pi} \right) \]  

(4.5)

Figure 4.2: (a) Turn-on and (b) turn-off energy losses of SCH2080KE by using FOD3180 gate driver. (c) Turn-on and (d) turn-off energy losses of SCH2080KE by using the gate driver in chapter 3. The measurements were collected with \( R_G = 10 \Omega \) and at room temperature in both cases.
The total losses in the six diodes were 11.4 W, while the turn-on energy loss of the diode consisted mainly of the reverse recovery energy.

For each diode, the turn-on losses can be estimated by $P_{\text{onD}} = E_{\text{onD}} \cdot f_{\text{sw}}$ which can be neglected. The turn-off losses of the diode have been neglected as well. In conclusion, each SiC-MOSFET will consume approximately $P_{\text{MOSFET}}=24.2$ W at an effective drain current of 15 A. This will lead to an efficiency of 99% at 25 ºC and 98.5% at 150 ºC; the previous values are valid in case of neglecting the driving losses of the power switches which are usually low.

### 4.2. Static Thermal Model and Heat-Sink Selection

As the power losses have been estimated, the second step is to choose the proper heat-sink, which allows the SiC-MOSFET to operate below the maximum junction temperature in order to protect the devices from overheating and damage. In addition, the heat-sink should keep the junction temperature at a specific level to keep the losses below the set loss level in the previous section. Therefore, the static thermal model of the VSI has been employed to give a rough idea regarding the required heat-sink and its characteristics. In the proposed design, a single forced-air cooled heat-sink, as shown in Figure 4.5.(a), has been chosen to fulfill this task. The six SiC-MOSFETs have been placed on the heat-sink, where three MOSFETs have been placed and fixed with clamps on each lateral side.

The thermal pad which has been chosen to isolate the drain plate of the SiC-MOSFET is (THINC33TO2472851755803) with 0.3 mm thickness and it is made of silicon with a thermal conductivity of 1.9 W/m.ºC, which can isolate the DC voltage up to 6 kV. Consequently, the static model as shown in Figure 4.3 has been investigated with the following initial conditions, which represent the conditions of operating in an automotive application environment, where the approximate ambient temperature is 80 ºC. Hence, the required thermal resistance between the sink to ambient should be equal to $R_{\text{bja}}=0.15$ ºC/W in order to avoid the increment of the junction temperature over the specified level, which was set to 120.5 ºC as explained in equations (4.6) to (4.8). In order to find the suitable heat-sink with the smallest possible size, a heat sink with a thermal resistance of 0.5 ºC/W is used, which was very hard to find, especially with the required size condition and with a natural convection cooling system.
The selected heat-sink was LMK 5 from Fischer Electronics, which has the following dimensions (width=5 cm, height=5 cm, length=7.5 cm) as shown in Figure 4.5(a). This heat-sink includes an axial fan, which needs 24 V as a power source in order to afford the required case-ambient thermal resistance as shown in Figure 4.3 The appropriate voltage level to drive the fan has been supplied from the output section of the topside gate driver. The obtained level of the case-ambient thermal resistance will be able to cool down the single SiC-MOSFET with total power losses (24 W) assuming constant power losses, which have been calculated in the previous section. The aforementioned level will ensure that the remaining junction temperature falls below the maximum junction temperature by 33 °C.

\[
T_{j,\text{MOS1}} = 175°C, \quad T_a = 80°C, \quad P_{\text{MOSFET1}} = 24W, \quad \theta_{jc,\text{MOS1}} = 0.44°C/W, \quad \theta_{cs,\text{MOS1}} = 0.35°C/W
\]

\[
\rightarrow \theta_{ca} = 0.5°C/W \rightarrow \theta_{ca} = 0.5 - 0.35 = 0.15°C/W
\]  

(4.6)

\[
\Delta T_{ca} = P_{\text{MOSFET1}} \cdot \theta_{cs,\text{MOS1}} + n \cdot P_{\text{MOSFET1}} \cdot \theta_{ca} = 30°C, \text{where } n = 6.
\]  

(4.7)

\[
\Delta T_{ja} = P_{\text{MOSFET1}} \cdot \theta_{jc,\text{MOS1}} + \Delta T_{ca} = 40.5°C \rightarrow T_j = 40.5 + 80 \cong 120.5°C
\]  

(4.8)

Where:

- \( T_a \): The ambient temperature 80 °C (Automotive Applications)
- \( T_{j,\text{MOS1}} \): The maximum junction temperature of the MOSFET without heat-sink
- \( \theta_{jc,\text{MOS1}} \): Thermal resistance between the junction and the case of the MOSFET
- \( \theta_{cs,\text{MOS1}} \): Thermal resistance between the case of the MOSFET and the sink
- \( \theta_{ca,\text{MOS1}} \): Thermal resistance between the case of the MOSFET and the ambient
- \( \theta_{sa,\text{MOS1}} \): Thermal resistance between the sink and the ambient
- \( P_{\text{MOSFET1}} \): The power losses in each MOSFET
- \( T_j \): The junction temperature of each MOSFET with heat-sink
4.3. EMI Modeling and Expectation in the Conducted Range

Considering the increment of the power electronic circuits in the various applications, many standards have been issued by the respective organizations in order to set the limits of electromagnetic interference EMI, which resulted from the power circuits. The permissible levels are different based on the application environments. The compliance to the EMI standards is known as the EMC; hence, the designed electronic circuits should comply with the set regulations. Therefore, different methodologies have been used throughout the literature to predict the EMI behavior of the power circuits before the construction phase in order to avoid the rejection of the produced circuits and designs in addition to reduce the cost and effort. EMI has been categorized into two main groups in the literature: the conduction and the radiated EMI. They are related to each other, whereas the conducted emission could cause a radiated EMI and vice versa due to the close positions of the EMI sources and victims. The conducted EMI is concerned with the electromagnetic propagation through the circuit network; the range of conducted EMI is defined to cover EMI frequencies up to 30 MHz.

The electromagnetic energy which is propagated in the air with frequencies higher than 30 MHz was defined in the literature by radiated EMI and it can be measured by an antenna which is connected to a spectrum analyzer. The test should be set up in a special isolated room in order
to concentrate on the main EMI source, other conditions regarding the height of the antennas and the measurement settings can be found in the standard and regulation documents.

The radiated EMI can be avoided by shielding the power circuit and cables and their effects in this case can be neglected. The major source of interference in the three-phase inverters, which has to be taken into account during the design, is the conducted EMI, which could disturb the behavior of the power circuit if it was not limited to a certain level. The dominant source of the conducted EMI is the slew rate of the voltage transitions during the switching and it becomes a serious problem if the voltage slew rate is higher than 10 kV/µs. Different methods have been used to limit the conducted EMI, such as using passive filters, which usually lead to an increase in the system size if the switching frequency is less than 20 kHz. The second possibility is to add a fourth leg in the designed inverter and this addition will result in increasing the system losses. One of the used methods to enhance the EMI behavior of the power inverter depends on proposing modified PWM techniques, as proposed in [62] and it will be presented in Chapter 5.

This method has been used to control the proposed design in order to enhance the EMI behavior and the system losses by minimizing the harmonics on the output voltages and currents. In addition to modifying the PWM control topology, the design depends on optimizing the circuit design, components positions and behavior of the driving and the power circuit.

The gate driver design includes a reduction in the voltage and current ringing during the switching by controlling the effective parameters and mainly the gate voltage and the gate resistor. Furthermore, it sets the slew rate at a specific level in order to enhance the EMI behavior during the switching. On the other hand, the power circuit has been designed to decrease the EMI without affecting the system performance. The EMI behavior of the proposed design has been practically investigated and compared with a simulation circuit, which has been constructed based on the physical layout of the power circuit PCB, assuming the inductive behavior of the PCB traces. One of the parameters which is considered during the modeling phase was the drain-heat-sink capacitance \( C_{dh} \). This capacitance is influenced by three parameters: the thickness of the thermal pad, the switching frequency and the flowing current level. The role of this capacitor appears during the PWM switching on the drain causing a pulsed current which flows through this capacitor; one of the proposed solutions to this issue is to connect the heat-sink to the negative terminal of the DC source.
4.3.1. Physical Layout Analysis

The traces behave like a pure resistor at low frequencies and it can be represented as pure inductance at high frequencies, within the conducted EMI range, due to the following equation.

\[ Z = R + j \cdot \omega \cdot L \]  \hspace{1cm} (4.9)

It can be noticed that at high frequencies, the PCB traces will behave as an inductor owing to the dominance of the frequency in the second part of the equation and in this case, the resistive part can be neglected. According to equations (4.10) and (4.11), the inductance of PCB traces and vias can be calculated. The model of the power circuit and the values of the inductances have been estimated based on the trace dimension as shown in Figure 4.4. The formula of the PCB trace inductance can be given as [63] by:

\[ L(\mu H) = 0.0002 \cdot X \cdot \left[ \ln \left( \frac{2X}{W+H} \right) + 0.2235 \cdot \left( \frac{W+H}{X} \right) + 0.5 \right] \]  \hspace{1cm} (4.10)

Where X, W and H represent the length of the trace, the width of the trace and the thickness of the trace; all dimensions in cm. In addition to the inductance, which results from the trace, an extra inductance usually result from the vias and the value of these inductances can be calculated by (4.11) as proposed in [63].

\[ L(nH) = \frac{h}{5} \cdot \left( 1 + \ln \left( \frac{4 \cdot h}{d} \right) \right) \]  \hspace{1cm} (4.11)

Where h representing the PCB thickness in mm and d representing the via’s diameter in mm.

The estimated values of the parasitic parameters in the proposed design have been discharged in Table 4.2.

<table>
<thead>
<tr>
<th>Parasitic Parameters</th>
<th>Parasitic Values in [nH], [pF]</th>
<th>Parasitic Parameters</th>
<th>Parasitic Values in [nH], [pF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>L+, L-, Lm1, Lm2</td>
<td>31.3, 123, 16, 15, 14.4</td>
<td>L2</td>
<td>14.6</td>
</tr>
<tr>
<td>Lm3, Lm4, Lm5, Lm6</td>
<td>43, 13.5, 11, 14.4</td>
<td>L51, L53, L55</td>
<td>6.8, 6.8, 6.7</td>
</tr>
<tr>
<td>Lm7, Lm8, Lm9, Lm10</td>
<td>15.1, 18.1, 17.3, 8.4</td>
<td>L22, L54, L56</td>
<td>22.7, 15.6, 25.3</td>
</tr>
<tr>
<td>Ls1b, Ls3b, Ls5b</td>
<td>22.7, 15.6, 25.3</td>
<td>Cout</td>
<td>175</td>
</tr>
<tr>
<td>Ls2b, Ls4b, Ls6b</td>
<td>7.9, 7.9, 7.9</td>
<td>L1a, L1v, L1b</td>
<td>28.5, 1, 17</td>
</tr>
<tr>
<td>Cdh1, ..., Cdh8</td>
<td>65</td>
<td>L2a, L2v, L2b</td>
<td>22.6, 1, 15.9</td>
</tr>
<tr>
<td>C1, C2, C3</td>
<td>4.7</td>
<td>L3a, L3v, L3b</td>
<td>22.6, 1, 14.4</td>
</tr>
</tbody>
</table>

Table 4.2: The parasitic parameters in the equivalent circuit of a three-phase inverter at high frequency
Figure 4.4: (a) The traces dimensions in the power circuit board (b) The equivalent circuit of a three-phase inverter in a high frequency domain
4.3.2. Parasitic Parameters of the Heat-Sink

The modeling of parasitic capacitances and especially for the drain-heat-sink capacitances, have been carried out based on the equations of the interconnection capacitance for VLSI circuit [64] and the results have been compared with an existing method in the literature [65]. This method will be verified for calculating the stray capacitance between the heat-sink and conducting drain-plate. The validity of the proposed method results from the similarity of existence of several conductors on a substrate with separation distances between the conductors and also between the conductors and the ground substrate. Consequently, the conditions of modeling the heat-sink and conducting plates are similar to the prior modeling methods, which mean the validity of applying (4.12). Based on the previous assumption, the stray capacitance per unit length of a single conducting plate on a heat-sink can be given by equation (4.12). Figure 4.5.(b) shows the analysis model of stray capacitances due to the heat-sink utilization.

\[
C_s = \frac{\varepsilon_r \cdot \varepsilon_0 \cdot W}{H} + 2.977 \cdot \varepsilon_0 \cdot \left( \frac{T}{H} \right)^{0.232} + \varepsilon_0 \cdot \left( \frac{0.229 \cdot W}{S} + 1.227 \cdot \left( \frac{T}{S} \right)^{1.384} \right) \cdot \left( \frac{H}{T} \right)^{0.398}
\]

\[
C_s(MOSFET) = 266 \text{ pF} \cdot \frac{2.1 \text{ cm}}{100 \text{ cm}} = 58.4 \text{ pF}
\]

Where \(\varepsilon_0\) is the free space permittivity and equals \(8.85 \times 10^{-12} \text{ F} \cdot \text{m}^{-1}\), \(\varepsilon_r\) is the relative permittivity of the insulation sheet and it equals 5.8, \(T\) is the drain plate thickness, \(H\) is the distance between the drain plate and the heat-sink, \(W\) is the width of the drain plate of the MOSFET and \(S\) represents the separation distance between the MOSFETs on the same side of the heat-sink.

The first term in the equation represents the capacitance between the conducting plate and the heat-sink. The second term represents the capacitances of the side wall of the conducting plate to the ground and the last part represents the capacitance between the conducting plates. Likewise, the stray capacitance between the bottom of the heat-sink and the PCB board as shown in Figure 4.6 can be given by:

\[
C_{h-g} = \frac{\varepsilon_0 \cdot A}{d} = 6.6 \text{ pF}
\]
Where $A$ is the bottom side area of the heat-sink, $d$ is the separation distance between the heat-sink and the PCB board. As a result, the total stray capacitance between the drain and the heat-sink can be estimated by (4.14).

$$C_T = C_s(MOSFET) + C_h-g \quad (4.14)$$

![Figure 4.5](image)

Figure 4.5.(a): heat-sink size (50mm, 50mm, 75mm) and the SiC-MOSFETs distributed on each side

The second method which was used to estimate the total drain-heat-sink is explained in [65] and it applies the theory of the analytical function of complex variables to the metallic plate ground electrostatic problem in order to estimate the stray capacitance of the heat-sink. The final equation of stray capacitance of the drain-heat-sink can be given by (4.15).

$$C_T = \frac{4 \cdot \varepsilon_r \cdot \varepsilon_0}{\pi} \cdot W \cdot \ln \left( \frac{Y}{H} \right) + \frac{A_d}{d} \cdot \varepsilon_0 \cdot \varepsilon_r + 0.88 \cdot \varepsilon_0 \quad (4.15)$$
The second term represents the capacitance between the heat-sink and the bottom side of the drain plate and $A_d$ represents the area of the drain plate. The last term represents the fringing fields near the edges of the conducting plate and it can be calculated based on the Schwartz-Christoffel’s transformations, this value can be neglected when the separation distance between the drain plates is large enough. Consequently, the total stray capacitance of the heat-sink has been estimated and its value was 65 pF. The result of the second method was approximately equal to the result of the first assumption.

4.3.3. Conducted EMI Measurements

The conducted EMI can be defined as the energy that propagates through the circuit cables, which connect the system to the source. The conducted EMI can also be formed in the interconnecting subsystems. This behavior will allow the interference signals to pass in conjunction with the main functional signal. This kind of interference is defined to have a dominance impact within a specific frequency range starting at few Hertz and ending at 30 MHz according to the EMC standards.

Recently, the attention to the EMI behavior in the power applications based on SiC devices has been noticed due to the promised fast switching capabilities in contrast to the Si devices. These higher switching speeds will lead to producing higher voltage slew rates; due to the influence of the generated parasitic parameters this will lead to increase the EMI. Therefore, this impact must be analyzed in order to confirm the compliance of the circuits, which use these devices according to the EMC standards and to check the filtering requirements. In this part, the typical and the used setups for measuring the conducted EMI will be addressed. The compliance of the resulted
EMI spectrum to EMC standards will be presented in Chapter 7. The aforementioned chapter will present an evaluation of the complete system in all the design aspects.

Typically, the conducted EMI can be measured using the Line Impedance Stabilizing Network, also known as LISN. The main task of the LISN is providing a 50 Ω in the direction of the inverter in order to pick up all the conducted EMI noises, which result from the power circuit. According to the EMC standards for measuring the conducted EMI CISPR 16, the LISN must be placed 80 cm far away from the power circuit in order to ensure the collecting of the noises within the conducted EMI range. In order to plot the power spectrum for the conducted EMI, the LISN must be connected to the spectrum analyzer as shown in Figure 4.7. In addition, the LISN and the heat-sink of the power devices must have the same ground in order to obtain accurate measurements. Furthermore, it is possible to measure the conducted EMI using other methods. One of these methods is the usage of active voltage probes such as R&S®ESH2-Z2, which have the ability to measure the conducted EMI from 0 dBμV and up 150 dBμV which corresponds to -120dB and up to 30 dB in the dB range. In this work, the ESL6 spectrum analyzer is used to draw the conducted EMI spectrum within the range of 9 kHz up to 30 MHz; the voltage probe approach has been used to fulfill this task considering the separation distance, which should be kept (more than 80 cm) between the device under test and the spectrum analyzer.
### 4.3.4. Simulated and Experimental EMI Spectrums

The final phase is to investigate the complete proposed model as shown in Figure 4.4, which has been implemented in LTspice IV using the values in Table 4.2. The EMI behavior within the conducted EMI range has been compared with the empirical results, which have been collected by the spectrum analyzer within the conducted EMI range. The simulated prediction has been compared with the experimental measurements and they have been depicted in Figure 4.8 in order to clarify the comparison. The experimental resonant points are matched well by the simulation, which indicate that the resonant points of the conducted EMI have been verified by the simulation results. A slight difference of up to 250 kHz has been noticed between the simulated and the experimental results this may return to the neglecting of the effect coupling inductances between the traces in addition to the effect of traces resistance on the EMI behavior within this range due to their comparable values to the trace inductances, which have been neglected in the proposed model. Within the range from 250 kHz up to 5 MHz, the results showed approximately the similar behavior, which means that the coupling inductive and trace resistances have a bigger influence when the resonance points are located within the frequency range lower than 250 kHz. It is worth mentioning that the used control topology is the carrier-based space vector PWM (CB-SVPWM) with a modulation index equal to one (M=1), which will be presented in Chapter 5. The modulation index also has an impact on the conducted EMI behavior, but it has no influence on the prediction process.

![Figure 4.8: Comparison between experimental and simulated conducted EMI spectrum up to 5MHz using CB-SVPWM with M=1.](image-url)
CHAPTER 5

5. Control Topologies

5.1. Introduction

Space vector pulse modulation (SVPWM) is a favored topology which can control power converters due to its remarkable advantages over the conventional PWM in terms of harmonics reduction, better utilization of the DC bus voltage and its suitability for variable frequency applications. For instance, in variable frequency applications, SVPWM is essential in order to simplify the control of the induction motors, which is considered as a non-straight forward issue; thereby, the usage of the SVPWM will ease their control.

SVPWM differs from the classical sinusoidal-width modulations in the complexity of switching time computations; it starts mainly by minimizing the three-phase representation to a two-phase system, which is known as alpha-beta transformation in order to estimate the switching times by creating a rotated reference vector. In the new plane, the aforementioned vector usually rotates with a speed corresponding to the frequency of the fundamental output voltage. The new plane is divided equally into six sectors so that each sector contains two boundary vectors that have been used to calculate the projection of the rotated reference vector on the sector’s borders. Hence, the turn-on and turn-off times can be calculated as in [66], [67], [68] and [69].
In this chapter; the proposed strategy will generate referential voltage signals which will be compared with a carrier like the SPWM in order to generate the SVPWM pulse patterns; the extracted reference signals will be formed based on the summation of the pulse widths during the rotation of the reference vector and they will be multiplied by the duration of the consistent sectors within the alpha-beta plane. Therefore, the pulse widths formulae in the initial phase will be extracted as an alternative to turn-on and turn-off times and then the produced reference signals will be compared to a carrier signal in the final phase in order to recover the required pulse widths on the output as in the classical SVPWM.

5.2. Simplified Two Levels Carrier Based SVPWM

The classical SVPWM relies on generating a rotating field vector which represents the output voltage in order to generate the switching pulses by calculating the turn-on and turn-off times within the different sector time. Therefore, this mission begins by simplifying the three-phase representation into a two-phase system by using the Clarke transformation; where, the normalized three-phase voltages to the DC input voltage $V_{dc}$ can be expressed by

\begin{align}
V_{an} &= \sin(\omega t) \\
V_{bn} &= \sin(\omega t + 2\pi/3) \\
V_{cn} &= \sin(\omega t + 4\pi/3)
\end{align}

(5.1)

(5.2)

(5.3)

Assuming balanced three-phase loads, the transformation can be simplified and expressed by (5.4) and (5.5), presuming that the power circuit of a two-level three-phase inverter consists of six switches which are distributed equally to three legs of the inverter so that each one will contain two complementary switches. Consequently, eight switching vectors (states) will divide the alpha-beta plane into six equal sectors with a 60° angle. Some of these sectors are in the same quadrant, whereas, the six active vectors $V_1$ to $V_6$ form a regular hexagon and the zero switching vectors $V_0$, $V_7$ are located in the zero as depicted in Figure 5.1 (a).

\begin{align}
V_{\alpha} &= (\sqrt{3}/2) \cdot V_{an} = 0.866 \cdot \sin(\omega t) \\
V_{\beta} &= (1/2) \cdot (V_{bn} - V_{cn}) = 0.5 \cdot \sin(\omega t + 2\pi/3) - 0.5 \cdot \sin(\omega t + 4\pi/3)
\end{align}

(5.4)

(5.5)
Accordingly, the pulse width of each phase leg \( x = a, b, c \) in all sectors has been calculated using equations (5.6) and (5.7), where the turn-on and off times have a special definition in the proposed method as shown in Figure 5.1 (b). The formulae of the turn-on and turn-off times in the different sectors have been taken from [70]; based on these equations, the pulse widths formula has been placed.

\[
T_{x,pulse} = T_{x,off} - T_{x,on} \quad (5.6)
\]
\[
T_{sw} = T_{x,off} + T_{x,on} \quad (5.7)
\]

In order to simplify the representation of the pulse widths in the complete alpha-beta plane, four groups of vectors have been defined, where each group consists of three different vectors which cover the corresponding quadrant and which will be used to form the pulse width equations. Although the preliminary derivation showed the necessity of four different groups, the simplified version still proved the ability to represent all the groups using the elements of group 1 due to the relation between the different groups as listed in Table 5.1.

As a result, the final pulse widths in the different sectors have been summarized in Table 5.2, where “sec” represents the sector and “Quad” represents the quadrant. The next phase is to
produce the reference voltage signals, this has been carried out by summing the multiplication of the pulse widths with the corresponding sector time periods for each phase as in (5.8).

\[
T_{Apulse} = T_{sw} \cdot [A_1 \cdot \text{sec}_1 + (A_1 + B_1) \cdot \text{sec}_2 \cdot \text{Quad}_1 - (A_2 + B_2) \cdot \text{sec}_3 - A_3 \\
\cdot \text{sec}_4 - (A_3 + B_3) \cdot \text{sec}_5 \cdot \text{Quad}_3 + (A_4 + B_4) \cdot \text{sec}_6 \cdot \text{Quad}_4 + A_4 \cdot \text{sec}_6]
\]  

(5.8)

*Table 5.1: Vectors groups in the different quadrants.*

<table>
<thead>
<tr>
<th>Quad 1</th>
<th>Quad 2</th>
<th>Quad 3</th>
<th>Quad 4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(A_1 =</td>
<td>V_{a\alpha}</td>
<td>+ (1/\sqrt{3}) \cdot</td>
<td>V_{b\beta}</td>
</tr>
<tr>
<td>(B_1 =</td>
<td>V_{a\alpha}</td>
<td>- (1/\sqrt{3}) \cdot</td>
<td>V_{b\beta}</td>
</tr>
<tr>
<td>(C_1 = (2/\sqrt{3}) \cdot</td>
<td>V_{c\gamma}</td>
<td>= \sin(\omega t + \pi/2))</td>
<td>(C_2 = C_4)</td>
</tr>
</tbody>
</table>

Seeing that (5.8) is not in the simplest form; the formula can be simplified by substituting the sinusoidal values of \(A_1\), \(B_1\) as in Table 5.1 and the same procedure is still valid for the other phases. Hence the reference voltage signals can be given by

\[
T_{Apulse} = T_{sw} \cdot [A_1 \cdot X + B_1 \cdot Y]  
\]

(5.9)

\[
T_{bpulse} = T_{sw} \cdot [-B_1 \cdot Z + C_1 \cdot X]  
\]

(5.10)

\[
T_{cpulse} = T_{sw} \cdot [-A_1 \cdot Z - C_1 \cdot Y]  
\]

(5.11)

Where \(X, Y\) and \(Z\) represent the effective sectors after constructing the reference waveforms and they are given follows

\[
X = [\text{sec}_1 + \text{sec}_2 + \text{sec}_4 + \text{sec}_6]
\]

(5.12)

\[
Y = [\text{sec}_2 + \text{sec}_3 + \text{sec}_5 + \text{sec}_6]
\]

(5.13)

\[
Z = [\text{sec}_1 + \text{sec}_3 + \text{sec}_4 + \text{sec}_6]
\]

(5.14)

In the same way as the sinusoidal PWM, the reference signals will be compared with a carrier signal with a switching frequency \(f_{sw}\), which represents the sampling frequency and equals the switching frequency. The carrier signal will have a peak value equal to \(2 \cdot T_{sw}\) to ensure the modulation in the linear zone. The previous comparison will result in generating the SVPWM switching pulses, which will be applied later to control the inverter switches.
Finally, the complete steps for generating a proposed SVPWM structure have been summarized in an algorithm, which starts from the desired output voltages and ends up with the pulse sequence for each phase.

![Algorithm Diagram]

**Figure 5.2: Proposed SVPWM generation algorithm**

**Table 5.2: Calculations of the pulses width in each sector.**

<table>
<thead>
<tr>
<th>Sector</th>
<th>$T_{A\text{ pulse}}$</th>
<th>$T_{B\text{ pulse}}$</th>
<th>$T_{C\text{ pulse}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$T_{SW} \cdot A_1$</td>
<td>$T_{SW} \cdot (-B_1 + C_1)$</td>
<td>$T_{SW} \cdot (-A_1)$</td>
</tr>
<tr>
<td>2 Quad1</td>
<td>$T_{SW} \cdot (A_1 + B_1)$</td>
<td>$T_{SW} \cdot (C_1)$</td>
<td>$T_{SW} \cdot (-C_1)$</td>
</tr>
<tr>
<td>2 Quad2</td>
<td>$T_{SW} \cdot (-A_2 - B_2)$</td>
<td>$T_{SW} \cdot (C_2)$</td>
<td>$T_{SW} \cdot (-C_2)$</td>
</tr>
<tr>
<td>3</td>
<td>$T_{SW} \cdot (-A_2)$</td>
<td>$T_{SW} \cdot (A_2)$</td>
<td>$T_{SW} \cdot (B_2 - C_2)$</td>
</tr>
<tr>
<td>4</td>
<td>$T_{SW} \cdot (-A_3)$</td>
<td>$T_{SW} \cdot (B_3 - C_3)$</td>
<td>$T_{SW} \cdot (A_3)$</td>
</tr>
<tr>
<td>5 Quad3</td>
<td>$T_{SW} \cdot (-A_3 - B_3)$</td>
<td>$T_{SW} \cdot (-C_3)$</td>
<td>$T_{SW} \cdot (C_3)$</td>
</tr>
<tr>
<td>5 Quad4</td>
<td>$T_{SW} \cdot (A_4 + B_4)$</td>
<td>$T_{SW} \cdot (-C_4)$</td>
<td>$T_{SW} \cdot (C_4)$</td>
</tr>
<tr>
<td>6</td>
<td>$T_{SW} \cdot (A_4)$</td>
<td>$T_{SW} \cdot (-A_4)$</td>
<td>$T_{SW} \cdot (B_4 + C_4)$</td>
</tr>
</tbody>
</table>
5.3. Simulations and Experimental Results

In the initial phase; an open-source simulation software called GeckoCIRCUITS, which has the capabilities to perform a fast simulation, has verified the validation of the proposed topology. Thus, the reference signal for each phase was implemented based on the formulae in (5.9-5.11), where $A_1$, $B_1$ and $C_1$ have been represented by sinusoidal signals. On other hand, $X$, $Y$ and $Z$ were represented by digital pulses with unit amplitude. According to the appropriate sectors which are included within $X$; the duty cycle of $X$ has been set to 66.6% and the frequency to 100 Hz in order to cover the required ones, while the duty cycle of $Y$ was set to 33.3% with the same frequency of $X$, but the output has been inverted. The last signal $Z$, which has been implemented by a NAND logic gate and its inputs were $X$ and inverted $Y$, is shown in Figure 5.3.

![Figure 5.3: X, Y and Z definitions and their active sectors](image)

The final step is to generate the switching pulses, which can be done by comparing the modulating signal (reference signal) with a triangular or a sinusoidal carrier signal as shown in Figure 5.4, which has an identical frequency, equals to the switching frequency. The positive and negative amplitude of the carrier signal is equal in magnitude to the double of the switching period magnitude ($2 \cdot T_{sw}$) to confirm the operation in the linear zone, in other words, the modulation index must be less than one. The comparison with the positive part of the carrier will generate the switching sequence of the top switches in each leg and the negative one is used with the bottom side switches. Based on the previous steps, the generated pulses out of the comparison have been applied to the switch control inputs. Hence, the output waveforms were formed at the load side as shown in Figure 5.5.
In fact, the generated reference signal seems like a function of the sinusoidal signal in addition to the rectangular third harmonic signal. In order to explain this, it is necessary to recall the Clarke transformation which is the responsible of generating the components of the space vectors. The harmonics of tripled orders may be added to the phase voltages without affecting the Clarke components and the value of the line-to-line voltages. Once this reference signal is formed, it can be replaced for the sinusoidal reference signal in SPWM. It is worth mentioning that the number of curves that can be used as reference signal for SVPWM is infinite, further details concerning the different possible shapes of the reference signals for SVPWM can be found in [71].

Similarly, the topology has been implemented in FPGA using LabVIEW 2014; the same procedures, which have been clarified previously in the simulation stage, have been applied to
FPGA. In addition, the simplicity of implementation of the proposed technique offers a high execution speed and low memory size requirements. The implementation has been carried out on the FPGA within a single-cycle time loop (SCTL), which means the execution speed is 25 ns owing to the clock speed, which was 40 MHz in the used FPGA. Proceeding from the necessity to validate the implemented code, FPGA output control signals have been applied to a three-phase inverter. Hence, the switching frequency has been set to 10 kHz and the fundamental frequency was set to 50 Hz.

![Diagram](image)

Figure 5.5: (a) The normalized output waveforms by (simulation) and (b) by (experiment). (c) Harmonic Analysis of phase current and (d) of line-to-line voltage at the same load conditions in table 4.1.
Figure 5.5 (b) depicts the experimental three-phase voltages, line-to-line voltage and three-phase currents, which agree with the simulation results in terms of the smooth output current, does usage and the total harmonic distortion. The amplitude of the output phase voltage can be controlled by changing the modulation index, which is defined as the ratio between the carrier and the reference signal like the SPWM.

In the proposed method; the modulation index with a unit magnitude corresponds to 0.866 in the classical SVPWM; in other words, the maximum output phase voltage will be \((2/3) \cdot V_{dc}\) and \(V_{dc}\) in case of the line-to-line voltage.

The effective output voltage of each phase is given by \(V_{dc}/\sqrt{3}\), while the effective line to line voltage is \(\sqrt{3}V_{dc}/\sqrt{3}\), which means better utilization of the DC input voltage and hence reducing the currents in the switches at the same power rating, leading to an enhancement of the inverter’s efficiency. The next step is to analyze the harmonic distortion in the generated waveforms by applying fast Fourier transform on the phase current and line-to-line voltage. The results of the harmonic analysis are depicted in Figure 5.5 (c) and 5.5 (d), where THD in the phase current was 1.2% and in case of the line-to-line voltage was found to be 5%. The analysis outcomes showed a low distortion in the output waveforms.

![Figure 5.6: Normalized three-phase currents trajectory in αβ plane.](image)
Moreover, the extracted results show a reduction in the magnitudes of the third, fifth and the seventh harmonics, which gives the proposed method one more advantage in variable frequency applications due to the reduction of undesirable effects of the odd harmonics on the loads. The odd harmonics in induction motors are considered as the responsible factor of generating extra heat on the motor side. Therefore, the proposed CB-SVPWM, the third harmonic injection and other control topologies have been proposed previously to handle this issue and to avoid these harmful harmonics.

The study is going further in analyzing the normalized trajectories of the output currents to show the accuracy of the output waveforms using the proposed structure. Figure 5.6 depicts a three-phase currents trajectory in αβ plane and it shows a circular behavior within the aforementioned plane due to the smooth sinusoidal current behavior in the time domain.

5.4. A New Method for Dead-Time Compensation in Carrier-Based PWM

The increased demand on high speed converters led to set several safety requirements during the converter operation. One of these converters is the three-phase inverter, which consists of three legs in order to generate the output voltage and currents. Each leg in the inverter consists of two complementary switches which must not switch simultaneously in order to avoid the short-circuit fault, which can lead to destroy the switches. Therefore, a tiny fraction of the switching period should be used between the switching sequences of the top and bottom switches in each leg of the inverter.

This portion of time is defined as the dead-time, which should be kept as low as possible due to its effect on the inverter performance [72]. The side effects of the dead-time are not limited to the increment of the conduction losses, but also it causes a decrement of the fundamental output component, which can reduce the inverter efficiency [73]. Moreover, the dead time can lead to increase the low-order harmonics on the converter outputs, which have negative effects on the load side.

The dead-time is related to the converter power factor and it is correlated with the switching speed. In other words, the dead-time can limit the maximum switching speed in the three-phase
inverter. Therefore, its effect should be compensated in order to exploit the involved switch capabilities. The relation between the dead-time and the switching speed in the three-phase inverter applications has been discussed in [74].

For the sake of compensating the dead-time in the three-phase inverter, different methods have been proposed in the literature, such as the utilization of the average value theory by summing the averaged lost voltage to the command voltage. In addition, PI-controller and detecting the directions of the power flow were also used to solve this issue; further methods can be found in the literature as in [75]. The previous methods clash with the difficulty of implementation and the requirements of measurement devices, especially in the methods which depend on measuring the direction of the power flow and the requirements of several digital-to-analogue converter DAC. In this paper, a new method to compensate the dead-time will be introduced and analyzed.

![Error due to the dead-time and Compensation of the dead-time error](image)

Figure 5.7: The effect of the dead-time and the dead-time compensation on the output pulses.
The proposed method depends on applying phase shifts on both, the carrier signal and the reference signal. The aim of applying the aforementioned phase shifts is to generate compensated signals which can deal with the effect of the dead-time on the generated control pulses.

The ideal pulses of the switching patterns are shown in Figure 5.7 at the bottom switches and the top switches in the same inverter leg, which should switch complementary to each other. The practice of the ideal switching patterns might destroy the inverter during the operation due to the short-circuit fault, which usually results from the simultaneous turn-on of both switches in the same leg; therefore, the dead-time should be considered to avoid this case. On the other hand, this will result in errors in the pulse pattern of the top and the bottom switches; these losses are denoted by loss and gain as shown in Figure 5.7. These errors can be accumulated and they might disturb the whole PWM process. In order to deal with this issue, the switching pattern must be modified to get rid of the unfavorable effects of the dead-time consideration. Therefore, the switching patterns will be modified so that the implementation of the dead-time on the modified pulses must lead to the actual patterns. These patterns appear exactly as the ideal pulses in terms of the width, the only difference between the two patterns is the compensation of the dead-time effect.

Figure 5.8: The proposed method to compensate the dead-time in CBPWM.
The modified pulse patterns of the complementary switches have been depicted as shown in Figure 5.7. The gain section has to be implemented in the pulse pattern of the top switch in order to substitute the loss portion which results from the dead-time consideration. On the other side, the loss section has to be implemented in the pulse pattern of the bottom side in order to get rid of the gain section which resulted from the dead-time implementation.

The targeted patterns will be obtained by shifting the original carrier signal and reference signals in an amount that correlates with the magnitude of the dead-time as shown in Figure 5.8. Despite the fact that the phase shift is very small in the case of the reference waveforms, it is still possible to be implemented on the FPGA. Consequently, the phase shifts of the reference signal $\theta$, and the carrier $\theta_c$ can be determined by applying (5.15) and (5.16).

$$\theta_r [\text{in degree}] = \frac{t_d}{T_r} \cdot 360^\circ$$ \hspace{1cm} (5.15)

$$\theta_c [\text{in degree}] = \frac{t_d}{T_{sw}} \cdot 360^\circ$$ \hspace{1cm} (5.16)

$T_r$ represents the period of the reference signal, $t_d$ represents the required dead-time and $T_{sw}$ represents the switching period. After applying these phase shifts on the carrier and the reference signals; the resulted output pulses from the classical comparison in the CB-PWM will have a phase shift $\theta_d$ approximately equals to the phase shift of the carrier $\theta_c$ due to the dominance of this portion during the comparison process in CB-PWM in contrast to the magnitude of the reference phase shift.

The resulted pulse pattern from the previous step will be used as the first input of the digital OR gate, while the second input represents the switching pattern which results from the comparison between the original carrier and reference signals without phase shifts.

The output of this digital operation will generate the modified compensated switching patterns, which will result in the actual pulse pattern after applying the dead-time. The complete steps of the proposed method are depicted in Figure 5.8 and it has been implemented on FPGA using LabVIEW 2014 to investigate the validation of the proposed approach as shown in Figure 5.9.
5. 4. 1. Experimental Results

In this part, the effect of implementing the dead-time in the three-phase inverter based on the SiC-MOSFET is presented by analyzing the voltage drop waveforms over the SiC-MOSFET during the inverter operation. The utilized control topology in this work is the CB-SVPWM, which will be introduced in this chapter.

It is worth mentioning here that the proposed compensating method is applicable in all CB-PWM topologies. In order to show the necessity of compensating the dead-time in CB-PWM and to discuss its effect, the voltage drop waveforms over the SiC MOSFET in the three-phase inverter application have been investigated in different cases, such as: the case of ignoring the dead-time, dead-time consideration and finally, the dead-time consideration and its effect compensation. This comparison aims at showing the resulted voltage spikes during the switching transition and the THD in each case. As a result of the high switching speed capabilities of the
SiC-MOSFETs and their low input capacitance, it was possible to apply the PWM signals without considering the dead-time, but this was resulting in generating voltage spikes reaching 40% up to 60% of the applied DC-link voltage as shown in Figure 5.10 (a). This can destroy the SiC-MOSFET devices, if they have been employed with DC-link voltages near to their breakdown voltage limits.

In this case, it is recommended to choose SiC-devices, which can withstand the double output voltage in three-phase inverter applications. Different possibilities might result from neglecting the dead-time, such as the distortion of the CB-PWM performance and the generation of high harmonic levels at the load side.

In case of neglecting the dead-time, the total harmonic distortion of the output phase voltage was higher than 59% and higher magnitudes of the odd harmonics were noticed as shown in Figure 5.10 (b). Therefore, the dead-time was considered in the next investigations step and the pulses of voltage drop over the SiC-MOSFET presented a better switching behavior with maximum voltage spikes up to 25% of the applied DC-link voltage as shown in Figure 5.10 (c).

The previous measurement was considering a dead-time of five microseconds. Consequently, the harmonic distortion has been improved and the THD of the output phase voltage was 22%, which means an enhancement of approximately 40% on the harmonic distortion due to the dead-time consideration as depicted in Figure 5.10 (d). The third harmonic showed the biggest reduction due to this consideration; this reduction was more than 60%. The final case which has been investigated in this part was the effect of compensating the dead-time over the switching performance and its effect on the output harmonics. The pursued method and the aims for compensating the dead-time were explained previously. Therefore, the proposed method was considered in the applied CB-PWM over the three-phase inverter. The results showed very low voltage spikes in the voltage drop pulses over the SiC-MOSFET with overshooting of less than 5% of the DC-link voltage as shown in Figure 5.10 (e).
Figure 5.10: Normalized voltage drop pulses over the switch on the DC-link voltage of the inverter and harmonic analysis of the output phase voltage in case of CB-PWM: (a) and (b) without applying dead-time; (c) and (d) with applied dead-time; and (e) and (f) with dead-time compensation.
On the other hand, the THD was slightly higher, approximately 27% as illustrated in Figure 5.10 (f). The output of compensating the dead-time was showing a tradeoff between the slight increment of the THD and the huge reduction of the overvoltage spikes, which are regarded as a dominant issue in the EMI perspective.

![Figure 5.11: The output phase voltage (left) and the phase current (right).](image)

### 5.4.2. Dead-Time Settings for SiC MOSFET in VSI Application

One of the aspects which must be considered during the implementation of the PWM are the settings of the required dead-time level, which usually depends on the switching times of the used power switches of the power circuit. In the case under study, the SiC-MOSFET showed a capability to switch very fast with a maximum rise time of 150 ns and with a fall time lower than 100 ns. Therefore, the dead-time in case of utilizing the SiC-MOSFET must be selected to be higher than 150 ns and it is better to be chosen as close as possible to this value, especially if the dead-time compensation strategies were not considered. On the other side, the compensation of the dead-time will lead to a reduction of the switching losses and the voltage-drop spikes, thereby enhancing the EMI behavior of the power inverter and the driven load. Figure 5.11 depicts the effect of the dead-time compensation on the output phase voltage and phase current waveforms.
The first study case was to consider 0.5 µs as the required dead-time margin; the normalized voltage drop of the SiC-MOSFET is shown in Figure 5.12 (top). The maximum overshooting was 30% of the applied DC-link voltage; and the resulted total harmonic distortion was 20.3%. The increment of the dead-time over the required certain level will lead to an increase in the output harmonics on the load; for instance, the increment from 0.5 µs to 1 µs was leading to increase the THD around 3% and also the voltage spikes on the SiC-MOSFET as shown in Figure 5.12 (bottom). In conclusion, different dead-time levels have been investigated based on the performance requirements; the selection was settled on 0.5 µs as the best dead-time level in CB-PWM for three-phase voltage source inverter based on 1.2 kV SiC-MOSFETs.
6. Faults Detection and Protection Design for Three-Phase Voltage Source Inverter

6.1. Introduction

The reliability of the three-phase inverter is one of the important topics that must be considered during the design of the inverter. This importance returns to the destructive impact of the faults which might occur in the power inverters, which can result due to the failure of the used power devices. Therefore, different methods in the literature have been proposed to ensure the device reliability during the converter operation. Some of those were depending on detecting and diagnosing the faults within a specific short time which will give the protection circuits the required time to respond before the system failure [76].

The fault detection process must be fast and accurate concurrently in order to avoid the postponed response of the protection circuit. The fault detection is possible by applying mathematical transformations, which can explain the behavior of the power devices during the operation as discussed in the literature. The drawback of this method is the slow detection response, which makes this approach suitable in the analytical stages. On the other hand, other methods were dealing with this issue by monitoring the response of the detection circuit based
on the voltage levels showing a fast response. In contrast, an increment in the required measurements was noticed in order to locate the faults.

In this chapter, the attention will be directed to the design of protection circuits which can deal with the common faults in the three-phase inverter. The detection speed as well as the response of the designed circuits has to be be fast in order to keep pace with the fast switching capabilities of the SiC-MOSFET, which represents the main component in the designed three-phase inverter in this work. The investigated faults, which will be covered in this part, are overvoltage protection, overcurrent, short-circuit and overtemperature faults. The hazards of these faults, the different proposed designs and how to deal with them have been surveyed in previous works as in [77], [78] and [79].

6.2. Overcurrent Fault Protection

Overcurrent is a fault which might occur during the inverter operation due to many reasons such as the breakdown of the insulation of the power PCB or from the wrong connection in the designed circuit. In addition, this fault can also result from the ground fault which happens in case of the breakdown of the insulation of the motor windings or eventually from the cross conduction which could occur during the switching transition between the top and bottom switches on the same leg [78].

The cross conduction can result from the inverter supplied with wrong control patterns or during the turn-on of the top switch with a high-voltage slew rate, which can lead to inducing current in the gate of the bottom switch due to the Miller capacitance effect. This effect will cause a short circuit on the DC-link and therefore, high current will flow through the power circuit which can last for a short or long term depending on the switching speed. In order to detect the overcurrent fault, a shunt resistor was used in the power circuit between the negative DC-link and the emitter side of the power switches.

The voltage drop across the shunt resistor will be transferred to the detection board through an external wire to be filtered in the next phase by $R_4$, $C_1$ as shown in Figure 6.1. The resulted signal will be amplified by a non-inverting operational amplifier with an amplifying factor of ten; this voltage level will be passed through two diodes, which are connected in series in order to
prepare this voltage level to be compared with a reference value. The reference value can be set in the proposed design by controlling the value of the resistor $R_2$.

The designed circuit will generate a trigger signal at the output as shown in Figure 6.2 when the effective current which passes through the shunt resistor exceeds the limit which has been set to 35 A in the case of the current fault.

![Circuit Diagram](image)

**Figure 6.1:** The designed overcurrent fault detection circuit and the threshold and maximum margins.

The voltage drop over the shunt resistor which is corresponding to this current level is 210 mV and this is equivalent to a reference voltage level $V_A$ of 1.78 V. Therefore, if the voltage drop over the shunt resistor exceeds this margin, the Schmitt trigger circuit will generate a trigger pulse at the output instantaneously after a very short blank time which will only last for a few microseconds.

The generated pulse will be transferred to the FPGA through digital input modules in order to switch off the drivers during the activated time of the generated pulse, if the fault has been repeated twice continuously, the drivers will be turned off until finding out and solving the fault
originator. The designed circuit which is illustrated in Figure 6.1 has been set to meet the previous specifications and the complete protection design which will handle the output pulses is denoted for the overcurrent in Figure 6.9 by C1.

![Graph showing overcurrent pulse](image)

**Figure 6.2:** The output pulse of the overcurrent detection circuit if the shunt resistor voltage exceeded 210mV threshold.

### 6.3. Short-Circuit Fault Protection

The short-circuit fault has common causes with the overcurrent fault as mentioned in the previous section, but this type of fault can be considered as the most dangerous fault which can occur during the inverter operation due to its ability to terminate the switches of the inverter. Consequently, the response of the detection and the protection circuit should be fast and intolerant with this fault. The controller in this case should behave in a very short time, i.e. several microseconds in order to turn-off the drivers until finding the sources of the malfunction, which can be physical reasons related to the power circuit, related to the driver circuit or in some cases related to the control sequences in addition to the previous faults which have been mentioned in the preceding section known as ground faults.

The designed circuit for short-circuit fault detection shares the preparatory phase and components with the overcurrent protection circuit. The accompaniment between the two circuit
ends at the denoted point O.C as shown in Figure 6.3. The voltage drop over the shunt resistor is the detection sensor in the power circuit. The margin for detecting the short-circuit fault in the proposed design is limited to 1.4 times of the rated current which is equivalent to an effective current of 48.3 A in the case of the SCH2080KE SiC-MOSFET.

The reference voltage level has also been set by choosing the value of R₂ exactly like for the overcurrent. This level for detecting the short-circuit fault is set to 2.5 V. Hence, if an exceeding of the voltage margin is detected, the Schmitt trigger circuit will generate a trigger signal at the output instantaneously.

The generated pulse as shown in Figure 6.4 will then be transferred to the FPGA in order to manipulate the error and to generate the suitable response. The interpretation of the short-circuit fault will lead to a turn-off of the driver circuits for the long term in order to find the fault sources. The circuit has been tested in case of exceeding the set margin, which is corresponding to a voltage drop over the shunt resistor of 290 mV as shown in Figure 6.4. The reaction of the
detection circuit was fast and the controller could respond within 25 ns to turn-off the driver circuits.

![Graph showing the output pulse of the short-circuit detection circuit if the shunt resistor voltage exceeded 290 mV threshold.](image)

Figure 6.4: The output pulse of the short-circuit detection circuit if the shunt resistor voltage exceeded 290 mV threshold.

### 6.4. Overvoltage Fault Protection

In this section, a protection circuit of the overvoltage fault has been designed; this type of fault usually occurs in the three-phase inverter due to various reasons, such as the effect of the parasitic parameters between the gate and the source in case of using the SiC-MOSFET, in addition to the switching speeds and the slew rates of the applied gate voltage, which have an impact on generating the overshoot peaks.

The importance of this type of detecting faults results from the necessity of protecting the power switches from the breakdown during the operation in three phase inverter applications. The used method to fulfill this task depends on sensing the DC-link voltage; this voltage will be transferred to the detection circuit and it will be minimized by the voltage divider resistors $R_4$, $R_5$, $R_6$ in order to obtain $V_B$ as shown in Figure 6.5 marked in green.
The resulted input voltage $V_B$ will be compared with a reference voltage $V_A$, if the maximum reference voltage has been exceeded. A low trigger pulse will be generated at the output of the detection circuit, which will be transferred to the FPGA for interpretation and to turn-off the gate drivers until the DC-link voltage retreats to the required DC-link voltage level. The maximum permissible voltage level in the proposed design has been set to 828V and the lowest margin to reactivate the gate drivers has been set to 795 V; the set voltage levels represent the margins of the recommended DC-link voltage.

The margins can be set in the proposed circuit by controlling the values of the voltage divider resistors $R_1$, $R_2$ and $R_3$ as shown in Figure 6.5. The overvoltage fault detection circuit was investigated by applying a voltage pulse pattern as depicted in Figure 6.6 in order to see the speed of the response, which revealed a very fast response within few nano seconds. The design was also succeeded in generating a high trigger signal when the DC-link voltage level reverted to the rated level as shown in Figure 6.6.
6.5. Overtemperature Fault Protection

The junction temperature is considered as one of the main parameters in the power devices due to the importance of this parameter in deciding the applications in which it can be used. Most of the Si devices were rated for a lower junction temperature up to 150 °C in contrast to 600 °C theoretically possible for the SiC devices. The effect of the junction temperature is not limited to the application type, but it also affects the power device losses, particularly the SiC devices which are considered as positive temperature coefficient devices.

Therefore, the temperature of the power devices in the three-phase inverter applications should be limited to a certain temperature level lower than the rated junction temperature in order to protect the power switches from the damage or fatigue. Moreover, the operations of the power devices below the rated margin will affect the maximum losses in the used applications. The high cost of the sensors and the difficulty of measuring the direct junction temperature resulted in adopting simplified methods which depend on measuring the case temperature by thermocouples or NTC resistors and analyzing the equivalent thermal network of the power circuit based on the total power devices losses in order to estimate the corresponding junction temperature.
In this work, an NTC resistor has been inserted in a hole in the heatsink. The location of the NTC resistor between the drain plate and the heat-sink was used to measure the case-sink temperature. The maximum case-sink temperature (NTC) was set to 100 °C which will correspond to a junction temperature of 125 °C based on the analysis of the thermal network of the three-phase inverter and the heat-sink in Chapter 4.

The selected value of the NTC resistor was 1 MΩ, which will become 38.2 kΩ at 100 °C, therefore the resulted input voltage $V_B$ will be compared with the reference voltage which was denoted by $V_A$ as shown in Figure 6.7. A low trigger pulse will be generated at the output of the detection circuit in case of the fault occurrence as shown in Figure 6.8. Similar to the other detection circuits, the trigger signal will be transferred to the FPGA controller in order to deactivate the driver of the SiC-MOSFETs in the inverter, or it can be used to activate other fans in some applications, which require using several cooling systems.

Figure 6.7: The designed overtemperature fault detection circuit and the threshold and maximum margins.
Finally, the protective response to the preceding faults will be performed by the FPGA using LabVIEW 2014 in order to activate and deactivate the gate drivers of the power switches in the three-phase inverter as shown in Figure 6.9. The activation is related to the fault detection by the proposed circuits which revealed fast responses which make them able to provide the FPGA controller with the required triggering signals in order to behave and avoid the damage which can occur due to the fault occurrence.

![Figure 6.8: The output pulse of the overtemperature fault detection circuit (red) if the NTC temperature exceeded the 100 °C margin (black).](image)

The required detection time was approximately 20 ns in most of the cases except in case of the overcurrent, which showed a blank time requirement around 3 to 5 micro seconds, which can be considered as permissible, predominantly with regard to the existence of the short-circuit fault detection, which is working in parallel with the overcurrent detection circuit in order to feedback the FPGA with two different perspectives for the flowing current through the power circuit.

The resulted digital pulses from the detection circuits can be transferred directly to the FPGA through the digital input modules. As a preliminary step, it is possible to set the required deactivation time of the gate driver by using timer ICs as in [79]. In this work, the NE555 has been used to set the deactivation time in case of the fault incidence. Figure 6.10 depicts the PCB board of the aforementioned fault detection circuits. The complete schematic of the designed fault detection and protection circuits is illustrated in the appendix.
Overtemperature Fault Protection

Figure 6.9: The complete protection design in case of fault detection.

Figure 6.10: The PCB board of the overcurrent, overvoltage, short-circuit and the overtemperature fault detection circuits.
7. **Evaluation and Analysis of the Complete System**

For the sake of evaluating the complete system, the results of the system parts will be addressed and evaluated in this chapter. The assessment process will include an evaluation of the gate driver in terms of the driving losses, the EMI behavior and the provided switching speed capabilities of the gate driver. Concerning the power circuit, the power losses in the power inverter will be analyzed and the estimated efficiency will be presented; moreover the effect of the constructed control topology and the dead-time consideration of the system efficiency as well as the EMI behavior and the total harmonic distortion will be addressed. Finally, the response time of the protection circuits will be evaluated.

### 7.1. Evaluation of the Gate Driver

Before starting the evaluation of the designed gate driver, the switching behavior of the SiC MOSFET will be presented and it will be compared with the datasheet values in terms of the rise time, fall time, turn-on delay and turn-off delay times in order to have an idea about the switching capabilities of the investigated SiC MOSFET. The settings and the conditions in addition to the extracted values based the double pulse test, are summarized in table 7.1.

In fact, the measured values of the investigated parameters were slightly higher than the values which have been provided by the datasheet. This difference results from the utilization of the
inductive load in the double pulse test settings in contrast to a resistive load in the datasheet test setups. Moreover, one of the dominant parameters that affects the switching behavior is the external gate resistance due to its impact on the capacitive time constant which is equally dependent on gate resistance and the input gate capacitance.

<table>
<thead>
<tr>
<th>Measurements conditions</th>
<th>Measured</th>
<th>Datasheet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load</td>
<td>Inductive Load L= 1200 µH</td>
<td>Resistive Load R_L=40 Ω</td>
</tr>
<tr>
<td>Applied gate voltage</td>
<td>20 V, 0 V</td>
<td>18 V, 0 V</td>
</tr>
<tr>
<td>External gate resistance</td>
<td>10 Ω</td>
<td>0 Ω</td>
</tr>
<tr>
<td>Rise time</td>
<td>45 ns</td>
<td>33 ns</td>
</tr>
<tr>
<td>Fall time</td>
<td>40 ns</td>
<td>28 ns</td>
</tr>
<tr>
<td>Turn-on delay time</td>
<td>37 ns</td>
<td>37 ns</td>
</tr>
<tr>
<td>Turn-off delay time</td>
<td>125 ns</td>
<td>70 ns</td>
</tr>
</tbody>
</table>

Table 7.1: Comparison between the measured and datasheet values of the switching characteristics

The method used to extract the required parameters from the switching waveforms is depicted in Figure 7.1, using the same approach that has been followed by the datasheet.

The next step in this evaluation study is to show the capabilities and the results of the proposed gate driver in comparison with the optical gate driver FOD3180. The specifications of both gate drivers in addition to the slew rates of the current and voltage during the turn-on and turn-off were summarized in Table 7.2.
### Evaluation of the Control and Dead Time Compensation Strategies

<table>
<thead>
<tr>
<th></th>
<th>Proposed gate driver</th>
<th>FOD3180</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Switching speed range</strong></td>
<td>Up to 500 kHz, 200kHz (exp.)</td>
<td>Up to 500 kHz</td>
</tr>
<tr>
<td><strong>Output voltage range</strong></td>
<td>25 V, -6 V</td>
<td>20 V, 0 V</td>
</tr>
<tr>
<td><strong>Turn-on</strong></td>
<td>$dV_{gs}/dt$ 400 V/µs</td>
<td>500 V/µs</td>
</tr>
<tr>
<td></td>
<td>$dV_{ds}/dt$ -30 kV/µs</td>
<td>-9.2 kV/µs</td>
</tr>
<tr>
<td></td>
<td>$dl/dt$ 1300 A/µs</td>
<td>150 A/µs</td>
</tr>
<tr>
<td></td>
<td>$E_{M, on}$ 872 µJ</td>
<td>2200 µJ</td>
</tr>
<tr>
<td><strong>Turn-off</strong></td>
<td>$dV_{gs}/dt$ -600 V/µs</td>
<td>-650 V/µs</td>
</tr>
<tr>
<td></td>
<td>$dV_{ds}/dt$ 19.7 kV/µs</td>
<td>29 kV/µs</td>
</tr>
<tr>
<td></td>
<td>$dl/dt$ -800 A/µs</td>
<td>-1200 A/µs</td>
</tr>
<tr>
<td></td>
<td>$E_{M, off}$ 168 µJ</td>
<td>281 µJ</td>
</tr>
<tr>
<td><strong>Oscillations level</strong></td>
<td>Lower</td>
<td>Higher</td>
</tr>
</tbody>
</table>

Table 7.2: Evaluation of the designed gate driver and a comparison with FOD3180 gate driver

In contrast to the FOD3180, the proposed gate driver offers an enhancement in terms of the switching losses. Moreover, the proposed gate driver provides a wider range of the output voltage during the turn-on and the turn-off, which fits with the required gate voltages of the SiC MOSFETs.

Furthermore, the gate driver showed a slightly slower slew rate than FOD3180 in order to compromise between the generated EMI in the power circuit and the switching losses. This reduction in the slew rate was around 20% during the turn-on which was close to 5% during the turn-off. The higher reduction during the turn-on resulted from the higher positive voltage level at turn-on around 20 V in contrast to approximately -1 V during the turn-off.

### 7.2. Evaluation of the Control and Dead Time Compensation Strategies

A new control strategy based on the SVPWM background has been put forward in this work and it was presented in Chapter 5. The aims of the proposed method are to increase the DC-link voltage utilization in contrast to the SPWM and to reduce the harmonic distortion in the output waveforms in contrast to the classical SVPWM and SPWM.
The increased utilization of the DC-link voltage can also be considered as an advantage of the proposed topology by controlling the modulation index of the carrier signal. Similarly to the SPWM, the modulation index represents the ratio between the carrier and the reference signal amplitudes and the generation of the switching sequences depending on the comparison between the carrier and reference signals and it differs in the number of switching pulses due to the significance of the modulation index in the proposed method. In other words, the modulation index with a unit magnitude corresponding to 0.866 in the classical SVPWM. Further details about the output waveform features and the effect of the proposed method on the total harmonic distortion can be found in Table 7.3.

<table>
<thead>
<tr>
<th></th>
<th>Proposed strategy</th>
<th>SPWM</th>
<th>Traditional SVPWM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum output phase voltage</td>
<td>$(2/3) \cdot V_{dc}$</td>
<td>$V_{dc}/2$</td>
<td>$V_{dc}/\sqrt{3}$, (Linear Zone)</td>
</tr>
<tr>
<td>Maximum Line-to-line voltage</td>
<td>$V_{dc}$</td>
<td>$\sqrt{3}V_{dc}/2$, at M=1</td>
<td>$V_{dc}$</td>
</tr>
<tr>
<td>THD in phase current</td>
<td>1.2%</td>
<td>Higher than 2.5%</td>
<td>1.5%</td>
</tr>
<tr>
<td>Normalized output phase voltage relative to SVPWM</td>
<td>1.15</td>
<td>0.866</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 7.3: Comparison between the proposed method and SPWM and classical SVPWM

The used method showed an increment in the utilization of the DC-link voltage, which can be noticed from the output phase voltage as mentioned in table 7.3. The effective output voltage of each phase can be given by $V_{dc}/\sqrt{8}$, while the effective line to line voltage was $\sqrt{3}V_{dc}/\sqrt{8}$. In addition, the maximum phase voltage was increased by 15%, in contrast to the classical SVPWM, which means better utilization of the DC input voltage and hence reducing the currents in the switches at the same power rating. This will lead to an enhancement of the inverter’s efficiency. Moreover, the proposed method showed a low THD (approximately 5%) of the line-to-line voltage, which complies with IEEE-519 standards for AC motors drive requirements.

One of the aspects, which influences the operation of the power inverter, is the dead-time due to its impact on the switching speed capabilities; therefore, its impact should be compensated. On the other hand, the proposed methods in the literature require much effort to fulfill this task for both the software and the hardware approaches. Therefore, a new method for compensating the dead-time in carrier-based PWM and setting the optimal dead-time for three-phase inverter based on SiC-MOSFETs has been proposed as presented in Chapter 5. In fact, the effect of the
dead-time compensation is not only limited to enhancing the THD and reducing the voltage spikes as presented in Table 7.4, but it also tends to influence the EMI behavior.

<table>
<thead>
<tr>
<th>Without dead-time implementation</th>
<th>With dead-time implementation and without compensation</th>
<th>With dead-time compensation</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD (Phase Voltage)</td>
<td>59.7%</td>
<td>22%</td>
</tr>
<tr>
<td>Maximum Normalized Voltage spike relative V&lt;sub&gt;DC&lt;/sub&gt;</td>
<td>40%</td>
<td>25%</td>
</tr>
</tbody>
</table>

Table 7.4: Comparison of the effects of neglecting the dead-time and dead-time consideration without compensation and the dead-time consideration with compensation on the THD and the maximum spike voltages

The next phase in this part is identifying the optimal dead-time, which fit with the SiC-MOSFET capabilities and leads to lower THD levels. The effect of the selected dead-time was investigated at different values, which were as follows: 0.5 µs, 1 µs and 5 µs. A comparison between the resulted THD and the maximum voltage spikes at these values is summarized in Table 7.5.

<table>
<thead>
<tr>
<th>THD at 5 µs</th>
<th>THD at 1 µs</th>
<th>THD at 0.5 µs</th>
</tr>
</thead>
<tbody>
<tr>
<td>27.7%</td>
<td>22.7%</td>
<td>20.3%</td>
</tr>
</tbody>
</table>

Table 7.5: Comparison of the THD at different dead-times without compensation

7.3. Power Losses and Estimated Efficiency Evaluation

A prototype sample of the power inverter was constructed to meet the design requirements; the switching losses were measured at the required conduction current, i.e. 15 A and the required DC-link voltage i.e. 800V, whereas, the conduction losses were extracted by applying \( (I_d^2 \cdot R_{ds(on)}) \) based on measuring the on-state resistance \( R_{ds(on)} \) at different junction temperatures. On the other side, the switching losses were measured and extracted from the double pulse measurement at the same DC-link voltage and the required current level. The specifications of the inverter have been presented in Chapter 4 and the layout in addition to the minimum heat-sink selection was discussed there. The conduction losses and the switching losses were
presented in detail in the same chapter and in this section the final results will be summarized as well as the estimated efficiency of the power inverter based on SiC MOSFETs as listed in Table 7.6.

<table>
<thead>
<tr>
<th>The Power Losses Contribution</th>
<th>The Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total switching losses</td>
<td>26.4 W</td>
</tr>
<tr>
<td>Total conduction losses</td>
<td>107 W</td>
</tr>
<tr>
<td>Total FWDs</td>
<td>11.4 W</td>
</tr>
<tr>
<td>Total losses in each MOSFET</td>
<td>24.2 W</td>
</tr>
<tr>
<td>Efficiency at 25 °C</td>
<td>≈99%</td>
</tr>
<tr>
<td>Efficiency at 150 °C</td>
<td>≈98.5%</td>
</tr>
</tbody>
</table>

Table 7.6: The measured losses and estimated efficiencies for the 16kW Inverter at switching frequency of 5 kH, I_D= 15A and at 25 °C.

The system efficiency has been evaluated by applying equation (7.1)

$$\eta\% = \frac{P_{in} - P_{loss}}{P_{in}} \cdot 100\%$$  \hspace{1cm} (7.1)

In the previous table; the driving losses were too small in milliWatt, which is why they have been neglected. The dominant contribution of the power losses resulted from the conduction losses, especially with elevated temperatures at the same switching frequency. On the other hand, the switching losses can become the dominant contributor in the power circuit if the switching frequency exceeds the f_{sw}= 20 kHz at the same conducted drain current.

The estimated efficiency of the power inverter at different temperatures and at a fixed switching frequency has been depicted in Figure 7.2. Furthermore, the estimated efficiency at different switching frequencies at the same temperature and conducted current has been depicted in the same figure. The efficiency decreased strongly in the case of increasing the switching frequency from 5 kHz up to 100 kHz, which results in a reduction of the system efficiency by 5%, while the efficiency reduction due to the temperature elevation was much lower. At the same switching frequency of 5 kHz, the reduction was around 0.4%.
7.4. The Compliance of the Power Inverter to the EMC Standards

The next phase, which must follow the design and construction of the power inverter, is to check its compliance to the EMC standards. The standards of the conducted EMI can be classified into two main groups; the first group is related to civilian standards and the second one addresses the military standards.

In this section, the civilian standards will be presented briefly, which contain several EMC commissions. One of the commissions whose standards have been distributed and accepted around the world is the International Electrotechnical Commission (IEC), which is divided into two groups; one of them is associated with the IEC 61000 standards, the second group represents the International Special Committee on Radio Interference (CISPR).

The last group released several EMC standards in order to fit with different application requirements as shown in Figure 7.3. The focus in this work will be on the IEC 61800-3 standards, which are dedicated to the conducted EMI limits in variable-speed electrical power drive systems.
The aforementioned standard will be used in this work to check the compliance of the conducted EMI to the EMC standards. In the literature, different methods have been used in order to suppress the EMI sources which have been discussed briefly in Chapter 4.

These methods have been satisfied during the design and implementation of the power inverter and they can be summarized as follows: optimizing the power circuit design and the gate driver position in order to suppress the effect of the source inductance and designing an active gate control by combining the switching speeds and the level of the emitted noises. The third method which has been used in this work is the proposal of a modified PWM strategy which leads to reduce the EMI and the output harmonics. Finally, the selection of the proper gate resistance has been carried out in order to reduce the current and voltage slew rates during the switching transition.

The measurement setups of the conducted EMI for the three-phase inverter have been presented in Chapter 4 and the power spectrum of the conducted EMI in the prototype power inverter was collected within the conducted EMI range which can be seen in Figure 7.4.
The results show the compliance of the EMI behavior of the power inverter to the IEC61800-3 standard through the whole conducted frequency range. Except for the frequencies lower than 200 kHz, the EMI level was in the range of 20 dB to 30 dB higher than the limit. It is important to mention here that the obtained spectrum has been gained without filtering efforts. In order to suppress the EMI within the range of 9 kHz and up to 200 kHz, we can use a small EMI filter to fulfill the complete compliance, or more efforts should be done in the direction of reducing the parasitic inductance and capacitance effects by optimizing the positions of the power devices and minimizing the resulted parasitic capacitances, which result from the utilization of the heat-sink.

7.5. The Evaluation of the Detection and Protection Circuits

This section presents an evaluation of the designed protection circuits which deal with the common faults, which might occur in the three-phase inverter based on the SiC-MOSFET. The detection speeds in case of fault occurrence will be presented. The targeted faults in this work were the overvoltage, overcurrent, short-circuit and overtemperature faults. The designed circuits aim at protecting the SiC MOSFET from failure and providing reliability to the power circuit as presented in detail in Chapter 6. A brief overview of detecting levels in the different detection circuits can be found in Table 7.7. The table shows the trigger levels at which the detection circuit will produce a response to fault occurrence and it shows the method used to detect the faults. For instance, in case of increasing the DC-link voltage higher than the threshold level,
which corresponds to 828 V, the detection circuit will generate an instantaneous response which can be interpreted by the FPGA in order to switch off the drivers until the DC-link voltage retrieves the accepted level of 795 V. Further details about the other circuits can be found in Chapter 6.

<table>
<thead>
<tr>
<th>Type of detection circuits</th>
<th>Trigger level</th>
<th>Detection method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overvoltage fault</td>
<td>$V_{DC\text{-link}} = 828$ V</td>
<td>DC-link voltage (voltage divider)</td>
</tr>
<tr>
<td>Overcurrent fault</td>
<td>$I_{\text{rms}} = 35$ A</td>
<td>Shunt resistor (voltage drop)</td>
</tr>
<tr>
<td>Short-circuit fault</td>
<td>$I_{\text{rms}} = 48$ A</td>
<td>Shunt resistor (voltage drop)</td>
</tr>
<tr>
<td>Overtemperature fault</td>
<td>$T_c = 100$ ºC</td>
<td>NTC resistor (voltage divider)</td>
</tr>
</tbody>
</table>

Table 7.7: The trigger levels and the detection methods in the designed faults detection circuits.

Certainly, the detection circuits should respond to the fault occurrence very fast in order to pace with the fast switching speed capabilities of the SiC-MOSFET. Therefore, the detection speeds and the requirements for a blank time before generating the proper response in the designed circuit have been summarized in Table 7.8.

<table>
<thead>
<tr>
<th>Detection circuits</th>
<th>Speed of response</th>
<th>Type of Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overvoltage fault</td>
<td>Instantaneous</td>
<td>Switch off the drivers if detected higher than threshold</td>
</tr>
<tr>
<td>Overcurrent fault</td>
<td>3 to 5 µs</td>
<td>Switch off the drivers during the activated pulse time</td>
</tr>
<tr>
<td>Short-circuit fault</td>
<td>Instantaneous</td>
<td>Long term turn-off until finding out error source</td>
</tr>
<tr>
<td>Overtemperature fault</td>
<td>Instantaneous</td>
<td>Long term turn-off or turn-on extra fans</td>
</tr>
</tbody>
</table>

Table 7.8: The speed of response and the type of response at different faults occurrences

The response speeds were instantaneous in all detection circuits except for the overcurrent fault which was considered as a tolerant fault in this design for a few microseconds and after that the FPGA should respond and deactivate the gate driver. The tolerance with this fault returns to the set threshold level, which represents no dangers on the SiC MOSFET and due to the existence of the detection circuit in case of a short-circuit fault. The idea of providing fast responses at the output of the detection circuits in case of other fault occurrences returns to their devastating effects on the power devices. Therefore, the response of the FPGA must be set to switch off the drivers until finding the error sources or to increase the number of cooling fans in the case of the overtemperature fault. Finally, the four detection circuits were designed to interact with FPGA in order to generate the proper actions and to prevent the SiC MOSFETs in the power circuit from probable failure.
8. Summary and Outlook

8.1. Summary and Outlook

In this chapter, a summary of the design requirements and design steps of the three-phase voltage source inverter prototype will be presented. The design was depending on the utilization of the SiC-MOSFET. Additionally, an outlook of this work will be presented throughout this chapter. The first step which should be considered during the optimization of the voltage source inverter design is the proper selection of the main component type, i.e. BJT, MOSFET, JFET, etc. Moreover, the background technology of the key components is necessary, i.e. Si, SiC, GaAs, GaN. The selection process is also dependent on the design requirements such as the switching speed, the rated power, the cost, the size, the weight, filtering requirements, etc.

In case of the efficiency of the power inverter to be the major concern in the required design, the selection process should consider the devices which have the lowest losses and the best switching behavior. In terms of the system size, the device with minimal thermal impedance should be selected in order to reduce the heat-sink size, hence reducing the system size. In this work, the selected technology which was involved in the design was the SiC-Technology; this returns to its superiority over the Si-Technology in terms of the device losses and the thermal capabilities. On the other hand, the EMI modeling and analysis of the power inverters based on the SiC-devices have been addressed throughout this work. The importance of this research field returns to the existence of several challenges which must be defeated in the case of utilizing the
SiC-devices, especially in the switching converters due to the generated oscillations within the switching waveforms which are usually created owing to the strong impact of the parasitic parameters in the power circuit. This influence is more dominant in SiC devices in contrast to Si devices.

Specifically, the investigated SiC-MOSFET in this work was SCH2080KE manufactured by ROHM. The SiC-MOSFET showed very good capabilities in terms of fast switching and it demonstrated good thermal impedance. In fact, the thermal impedance of the SiC-MOSFET is dependent on the packaging type.

Furthermore, investigations of the static and dynamic electrical characteristics of the SiC MOSFET and a behavioral study of the channel mobility with variant temperature were fulfilled. The study of the channel mobility was depending on the measurements of the transconductance and the other electrical characteristics of the SiC-MOSFET, exploiting the relationship between the channel mobility and the transconductance in the pinch-off region. The investigations of the SiC-MOSFET characteristics led to a better understanding of the gate driver design and the requirements.

The design of the gate driver for the SiC-MOSFET has to be considered as a compromise between the switching capabilities of the SiC-MOSFETs and their EMI behavior due to the proportional relationship between the switching frequency and the EMI behavior. In other words, the EMI increases due to the fast slew rates of voltage and current during the switching transition.

On the other hand, the oscillations within the switching waveforms are usually formed due to the impact of the parasitic parameters in the power circuit. Consequently, the design of the gate driver should consider the aforementioned issues by selecting the proper tradeoff between the switching speed and the required slew rate of current and voltage drop during the switching transition.

Furthermore, the design of the SiC-MOSFET gate drivers was presented considering the effect of several design parameters, such as the selection criterion of the gate driver components based on the driven load and its current and voltage specifications. The proposed driver could
switch the SiC-MOSFET up to 200 kHz without distortion on the duty cycle. The operating switching frequency in this work has been set to 5 kHz, which is enough to fulfill the tradeoff between EMI and the switching losses for electric vehicle applications.

The designed gate drivers were employed to drive a prototype of a three-phase voltage source inverter, which is dedicated to EV applications. The proposed design depends on driving the SiC-MOSFET at a specific operating point which corresponds to minimum conduction losses. The efforts were mainly focused on the reduction of the conduction losses due to their big influence on the system efficiency and their huge portion in the total losses for switching frequencies lower than 20 kHz. The minimization of the switching losses and the EMI behavior have been considered in the designed power inverter during the gate driver phase by selecting the proper control parameters of each step individually and integrally. In addition, a new control topology and new dead-time compensation methods, which have been presented in this work, played a role in suppressing the generated EMI by reducing the oscillations and the peaks in the voltage drop pulses.

The EMI behavior of the power inverter is an essential issue which must be considered during the design phase in order to avoid the rejection of the product in case of incompliance to the EMC standards and regulations. These regulations have been set by different organizations around the world in order to regulate unwanted radiation and the conduction of the electromagnetic waves between the EMI sources and victims to prevent possible malfunctions. Hence, it is necessary to check the compliance of the product with the EMC standards before the manufacture phase.

The EMI behaviors of the voltage source inverters have been introduced in this dissertation depending on analyzing the physical layout of the power inverter PCB considering the effect of the generated parasitic inductances from the PCB traces and the inductance of the via. The analysis was going further by investigating the parasitic capacitances which are generated between the different drain plates on the same side of the heat-sink, defined as fringing effect. Moreover, the parasitic capacitance between the drain plates and the heat-sink have been considered. The determination of parasitic capacitances values was inspired by the identification of the interconnection capacitances in VLSI circuits due to the similarity in both cases.
One of the effective design parameters in the physical aspect is the selection of the proper cooling technology. The used cooling technology can result in minimizing the size of the heat-sink, especially if the size is a crucial design issue as in the EV. The chosen cooling technology in this work was the forced-air cooling with a small heat-sink profile (W=5 cm, H=5 cm, L=7.5 cm). The cooled air is coming from a fan which requires a 24V power supply to be supplied from one of the final stages of the high side driver PCB circuit. It is worth mentioning that the selection of the heat-sink was performed based on the static thermal network of the power circuit.

The optimization disciplines of the three-phase inverter are very wide and varied; some of these disciplines have been summarized in this dissertation in the block diagram which has been depicted in Chapter 1. The control perspective represents the implemented control topology which can be SPWM, SVPWM and CB-SVPWM, etc., and it is considered as one of the key parameters, which has an influence on the inverter performance. In this dissertation, a new and simplified CB-SVPWM has been created to reduce the implementation complexity of the SVPWM-topology and to show the effect of the control topologies on the system efficiency and the quality of the output voltages and currents.

Three reference signals have been used to retrieve the switching patterns of the SVPWM for the two-level voltage source inverter. The proposed method showed lower harmonics in the phase currents and voltages in contrast to the other control topologies in addition to the simplicity of the implementation and the speed of the calculations with 25 ns. In fact, there is a hidden link between control topologies and the efficiency in three-phase inverters, which can be clarified by the effect of used control topology in increasing the maximum and the effective levels of the output phase-voltages and currents as in the SVPWM, which will lead to an increase in the final system efficiency by enhancing the utilization of the DC-link voltage. In the proposed control topology, it is possible to control the effective output voltage by controlling the modulation index; this increment has a drawback which is represented in increasing the THD on the output waveforms.

The implementation of the control patterns in the three-phase voltage source inverter has to consider a short time during the switching exchange between the top and the bottom switches in the same leg in order to avoid the short circuit faults and to reduce the harmonics in the output waveforms. The implementation of the dead time is necessary, but it can destroy the complete
PWM patterns due to the resulted reduction in the pulse widths and the shifted output pulses. Therefore, it is important to compensate the effect of the dead-time implementation, which has been proposed and investigated in this dissertation. The proposed method has been developed to be applied on all carrier-based PWM.

The last design issues that have been considered in this dissertation are the diagnosis and the protection of the three-phase inverter from the common faults. The designed circuits dealt with overcurrent fault, the short-circuit fault, the overvoltage fault and the overtemperature fault. The control topologies, dead-time compensation and the protection response have been implemented in this work on FPGA using LabVIEW 2014, which led to a high speed response and faster implementation speed.

According to the aforementioned results, the utilization of the SiC-MOSFET in the three-phase voltage source inverter, seems promising and it can result in very high-efficiency systems which correlate with the rated power of the designed inverter. In the proposed design, the resulted efficiency can reach up to 99%. The aforementioned facts are true if the challenges which have presented in this dissertation, have been defeated. The reliability of the SiC devices in power applications and the design challenges, which have been discussed within this chapter keep the doors open to induce the researchers’ curiosity to drive the SiC-technology to the desired maturity.
Appendix

Illustration 1: (a) The datasheet of the SCH2080KE (Page 1).
### Thermal resistance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal resistance, junction - case</td>
<td>$R_{thJC}$</td>
<td>0.44 to 0.57</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal resistance, junction - ambient</td>
<td>$R_{thJA}$</td>
<td>- 50</td>
<td>°C/W</td>
</tr>
<tr>
<td>Soldering temperature, wavesoldering for 10s</td>
<td>$T_{solder}$</td>
<td>- 265</td>
<td>°C</td>
</tr>
</tbody>
</table>

### Electrical characteristics ($T_A = 25^\circ$C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain - Source breakdown voltage</td>
<td>$V_{BRDSS}$</td>
<td>$V_{GS} = 0V, I_D = 1mA$</td>
<td>1200</td>
<td>-</td>
</tr>
<tr>
<td>Zero gate voltage drain current</td>
<td>$I_{DSS}$</td>
<td>$V_{GS} = 1200V, V_{GS} = 0V$</td>
<td>- 20</td>
<td>400</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_J = 25^\circ$C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_J = 150^\circ$C</td>
<td>- 170</td>
<td></td>
</tr>
<tr>
<td>Gate - Source leakage current</td>
<td>$I_{GSS}$</td>
<td>$V_{GS} = +22V, V_{DS} = 0V$</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>Gate - Source leakage current</td>
<td>$I_{GSS}$</td>
<td>$V_{GS} = -6V, V_{DS} = 0V$</td>
<td>-</td>
<td>-100</td>
</tr>
<tr>
<td>Gate threshold voltage</td>
<td>$V_{GS(th)}$</td>
<td>$V_{GS} = V_{GS}, I_D = 4.4mA$</td>
<td>1.6</td>
<td>4.0</td>
</tr>
<tr>
<td>Static drain - source on - state resistance</td>
<td>$R_{DSS(on)}$</td>
<td>$V_{GS} = 18V, I_D = 10A$</td>
<td>- 80</td>
<td>117</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_J = 25^\circ$C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_J = 125^\circ$C</td>
<td>- 125</td>
<td></td>
</tr>
<tr>
<td>Gate input resistance</td>
<td>$R_D$</td>
<td>$f = 1MHz$, open drain</td>
<td>- 6.3</td>
<td>-</td>
</tr>
</tbody>
</table>
### Electrical characteristics (T_A = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transconductance</td>
<td>g_m</td>
<td>V_DS = 10V, I_D = 10A</td>
<td>-</td>
<td>3.7</td>
<td>-</td>
<td>S</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>Cssé</td>
<td>V_DS = 0V</td>
<td>-</td>
<td>1850</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>Cssé</td>
<td>V_DS = 800V</td>
<td>-</td>
<td>175</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Reverse transfer capacitance</td>
<td>Crss</td>
<td>f = 1MHz</td>
<td>-</td>
<td>20</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Turn - on delay time</td>
<td>t_{(on)}</td>
<td>V_DS = 400V, V_GS = 16V</td>
<td>-</td>
<td>37</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Rise time</td>
<td>t_r</td>
<td>I_D = 10A</td>
<td>-</td>
<td>33</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Turn - off delay time</td>
<td>t_{(off)}</td>
<td>R_L = 40Ω</td>
<td>-</td>
<td>70</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Fall time</td>
<td>t_f</td>
<td>R_G = 0Ω</td>
<td>-</td>
<td>28</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Turn - on switching loss</td>
<td>E_on</td>
<td>V_DS = 600V, I_D = 10A</td>
<td>-</td>
<td>218</td>
<td>-</td>
<td>μJ</td>
</tr>
<tr>
<td>Turn - off switching loss</td>
<td>E_off</td>
<td>*E_off includes diode reverse recovery</td>
<td>-</td>
<td>64</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

### Gate Charge characteristics (T_A = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total gate charge</td>
<td>Q_G</td>
<td>V_DS = 400V</td>
<td>-</td>
<td>106</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>Gate - Source charge</td>
<td>Q_S</td>
<td>I_D = 10A</td>
<td>-</td>
<td>27</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Gate - Drain charge</td>
<td>Q_D</td>
<td>V_DS = 18V</td>
<td>-</td>
<td>31</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Gate plateau voltage</td>
<td>V_GS</td>
<td>V_DS = 400V, I_D = 10A</td>
<td>-</td>
<td>9.7</td>
<td>-</td>
<td>V</td>
</tr>
</tbody>
</table>

*1 Limited only by maximum temperature allowed.
*2 PW ≤ 10μs, Duty cycle ≤ 1%
*3 Pulsed
Illustration 2: The designed three-phase inverter prototype.
Illustration 3: The implementation of the proposed control topology and the dead-time compensation on the FPGA by LabVIEW 2014.
Illustration 4: The schematic of the faults detection and protection circuits.
Illustration 5: The implementation of the proposed control topology by GeckoCIRCUITS simulation software.
References


Versicherung

Hiermit versichere ich, dass ich die vorliegende Arbeit ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfs-mittel angefertigt habe; die aus fremden Quellen direkt oder indirect übernommenen Gedanken sind als solche kenntlich gemacht.


Die Arbeit wurde bisher weder im Inland noch im Ausland in gleicher oder ähnlicher Form einer anderen Prüfungsbehörde vorgelegt.

Hani Muhsen, Chemnitz, den 10.11.2015
1. The channel mobility behavior of the SiC-MOSFET with temperature variation is a controversial topic due to its dependency on the doping concentration in the power device. This behavior was analyzed by exploiting the relationship between the transconductance, the threshold voltage and the effective channel mobility at different temperature levels.

2. SiC-MOSFET has several driving requirements, which differ from the traditional Si-MOSFET in terms of the needed voltage levels, the offered switching speed capabilities, and their influence on the EMI behavior.

3. New trends in gate driver design for the SiC-MOSFET applications are pushing to provide high switching speeds capabilities and to reduce the effect of the parasitic parameters due to their impact on the resulted EMI, especially at elevated switching frequency speeds i.e. several hundred kilos Herz.

4. The power inverter is a key design parameter in electric vehicle applications. This returns to the lack of power supplies in these applications, i.e. the battery. Moreover, the limitation on the inverter volume, which includes the power circuit, the cooling system, and the filtering requirements, was leading to investigate the utilization of new semiconductor technologies such as the SiC and mainly SiC-MOSFET in order to exploit their benefits in terms of reducing the power devices' losses and reducing the cooling system size.

5. SiC MOSFET is confronted with several challenges such as the resulted oscillations due to the side effect of the parasitic parameters during the switching. Furthermore, the reliability of the power device in the long-term is still under investigation.

6. The involvement of the SiC-MOSFET as the basic component in the power inverter applications will lead to enhance efficiency of the system up to 99% at switching frequency of 5 kHz and junction temperature of 25 °C due to its low losses, which dominantly dependent on the operating switching frequency, junction temperature and the required output current and voltage levels. In addition, the usage of the SiC-
MOSFET can lead to reduce the size of the cooling system in contrast to the utilization of the Si-Technology.

7. The analysis of EMI behavior of the power inverter is necessary in order to investigate their compliance to the EMC standards which can stand in front of the validation of the design in case of their noncompliance to these standards. Hence, the EMI behavior of the power circuit must be analyzed in advance before the manufacturing step in order to reduce the costs and efforts; these targets can’t be fulfilled accurately without utilizing expensive commercial software.

8. It was found that the analysis of the EMI behavior of the power circuit in the physical layer level can lead to comparable results with the experiments due to the consideration of the traces and via’s and the heat sink effects during the analysis.

9. The similarity between the estimation of the parasitic capacitance that resulted from the usage of the heat-sink and the estimation of the capacitance in VLSI circuit, can be exploited to find the parasitic capacitance of the heat-sink and to investigate its influence on the generated EMI.

10. Space vector pulse modulation (SVPWM) is one of the favorite control methods in power inverter application due to their benefits over than the SPWM in terms of the lower THD and the utilization of the DC-link voltage, but this method requires high computations and sometimes difficulty in implementation. Therefore, a new control method based on the classical SVPWM was proposed, which is characterized by the implementation simplicity and the low computations’ requirements, and lower THD on the load side in addition to boost the utilization of the DC link voltage.

11. Compensating the effect of the dead-time in control topologies is necessary for reducing the overvoltage spikes on the power devices during the switching. This can lead to exploit the power device capabilities by operating them in voltage levels near to their rated blocking voltage considering a lower margin up to 10% maximum in contrast to 30% in case of neglecting the compensation of the dead-time effect.
12. The selection of the proper dead-time level considering the utilized power devices in the power circuit can lead to enhance the THD on the load and to reduce the overshooting over the power devices. This issue can be fulfilled as a compromise between the THD and the overshooting voltage.

13. The implementation of protection circuits and their responses to these faults must be very fast, which were instantaneous in the implemented circuits. It was found that the utilization of the FPGA in order to compile these faults, and the proper settings of the detection circuits can lead to protect the power inverter and ensure their reliability.
Curriculum Vitae

Summary

Hani Muhsen was born in Jordan on December 04, 1982. He received the Bachelor of Engineering in Electrical Engineering from Palestine Polytechnic University in 2005 with excellent evaluation. In 2009, he received M.Sc. in Electrical Engineering from Jordan university of Science and Technology with very good evaluation. He is currently a PhD student in the chair of Power Electronics and Electromagnetic compatibility, and he worked as “Teacher Assistant” in Palestine Polytechnic University during (2005-2006). From 2008 to 2011; he worked as “Technical Electronic Instructor” in Wadi Alseer Technical College, Amman, Jordan. He obtained a German Academic Exchange Scholarship (DAAD) for studying M.Sc. during (2006-2009) and for PhD study since Feb. 2013.

Experience

Feb.2013-Feb.2016 Technical University of Chemnitz [Technische Universität Chemnitz] Chemnitz, Germany
PhD Student

Technical Instructor

Sep.2005-July 2006 Palestine Polytechnic University Hebron, Palestine
Teacher Assistant

Education

Sep.2006- Sep.2009 Jordan University of Science and Technology Irbid, Jordan
MSc. in Electrical Engineering (Very Good)

Sep.2000- June 2005 Palestine Polytechnic University Hebron, Palestine
BEng. in Electrical Engineering (Excellent)
Scholarships

German Academic Exchange Service (DAAD) award to complete the Master (2006-2009).

German Academic Exchange Service (DAAD) award to Learn German Language, 2011 (6 months).

German Academic Exchange Service (DAAD) award as a researcher (2012- Feb.2016).

Publications

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<tr>
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<tr>
<td>Sep.-2015</td>
<td>Three Phase Voltage Source Inverter Using SiC MOSFETs; Design and Optimization</td>
<td>EPE ECCE Europe, 2015</td>
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<tr>
<td>May-2015</td>
<td>A New Simplified Space Vector PWM Scheme for Two-Level Voltage Source Inverter</td>
<td>PCIM Europe, 2015</td>
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<td>May-2015</td>
<td>Design and Evaluation of Gate Drivers of SiC MOSFET</td>
<td>PCIM Europe ,2015</td>
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<td>May-2015</td>
<td>Comparison of drivers for SiC-BJT, Si-IGBTs and SiC-MOSFETs (Coauthor)</td>
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