Process Window Challenges in Advanced Manufacturing: New Materials and Integration Solutions

Robert Fox, Rod Augur, Craig Child, Mark Zaleski
GLOBALFOUNDRIES/Technology Development and Yield Engineering
400 Stonebreak Road Extension, Malta, NY, 12020, USA
robert.fox@globalfoundries.com

Abstract
With the continued progression of Moore’s law into the sub-14nm technology nodes, interconnect RC and power dissipation scaling play an increasingly important role in overall product performance. As critical dimensions in the mainstream Cu/ULK interconnect system shrink below 30nm, corresponding increases in relative process variation and decreases in overall process window mandate increasingly complex integrated solutions. Traditional metallization processes, e.g. PVD barrier and seed layers, no longer scale for all layout configurations as they reach physical and geometric limitations. Interactions between design, OPC, and patterning also play more and more critical roles with respect to reliability and yield in volume manufacturing; stated simply, scaling is no longer “business as usual”. Restricted design layouts, prescriptive design rules, novel materials, and holistic integration solutions each therefore become necessary to maximize available process windows, thus enabling new generations of cost-competitive products in the marketplace.

1. Introduction
Logic device scaling to and beyond the 14nm technology node has seen accelerated erosion of overall integrated back-end-of-line (BEOL) process windows due to the growing importance of total process variation relative to feature size. As one example, the difference in process window between a 64nm-pitch via integrated to full theoretical process assumptions and the same via upsized for reduced resistance is highlighted in Monte Carlo simulations in Figure 1. In the ideal case, there exists a 4-sigma confidence level for via-to-metal spacing above the minimum requirement for reliability. However, when via size is intentionally increased (e.g. for improved performance or yield), process window is reduced to an unacceptable 2-sigma. In order to achieve a minimum 3-sigma process while maintaining the larger via, all other possible sources of in-line variation (e.g. CD and overlay) must be very tightly controlled – each to their maximal capabilities. With all in-line controls pushed to fundamental metrology or equipment limits, the only avenue back to a larger integrated process window is by reduction of via size back toward the original, ideal process. For some unit processes, e.g. traditional PVD barrier, performance scaling is all but entirely halted below 30nm width due to the need to maintain minimum thickness at via bottom and sidewall for yield and reliability. For others, e.g. reactive ion etch, scaling becomes increasingly challenged by the simultaneous requirements of reduced dielectric damage (i.e. undercut/profile control) for yield and integrated dielectric constant (i.e. capacitance) for performance. As such, total integrated process windows at product-level can routinely span only a few nanometers for selected design systematics prior to or without significant optimization (illustrated in Figure 2). To truly expand process window (and thereby allow continued BEOL scaling), multiple simultaneous
solutions become required from design (e.g. restricted layouts, prescriptive design rules, templated designs), unit process (e.g. novel metallic and dielectric materials), and process integration (e.g. self-aligned double- and quadruple-patterning).

2. Discussion
2.1 Design
Several approaches to process window enhancement have been evaluated in design, ranging from entirely upfront to opportunistic post-processing. Each path must delicately balance tradeoffs in process margin and time-to-market; ultimately, choice of architecture depends strongly upon cooperation between design and process teams. Design layout restrictions (e.g. unrestricted versus partially- and heavily-restricted layouts, as shown in Figure 3) have been extensively explored, especially for lower metal levels where tradeoffs in area, track utilization, and pin count are most important. Partial router restrictions can greatly reduce metal complexity while also maximizing metal line end extensions (LEE) – both known to be critical for yield - without penalty. More extensive restrictions can further improve counts of minimum LEE (as highlighted in Figure 4), but at the cost of extra metal layers (i.e. additional cost through added mask count and additional processing). Replacement of bi-directional with entirely unidirectional layout in M1, for example, can allow for very high pin accessibility and unidirectional routing in M2 (and above), which greatly increases process window due to reduced complexity and therefore fewer design-sensitive systematics. Unidirectional layout can also allow the use of LELE or SADP process integrations (see section 2.3) instead of LELELE with more complex tolerances. However, tip-to-tip spacing becomes highly-constrained, and a purely unidirectional M1 layout can cause cell-cell placement violations. In those cases, preferred orientation (as opposed to pure unidirectional) can provide relief.

The use of prescriptive design rules is another, less intrusive approach to layout restriction. To enable such rules, simulations of areal images from known, sensitive layout constructs are performed. Cumulative analysis of individual contributions is used to set upper specifications of PV (Process Variation) bandwidth over a range of critical layout constructs, which in turn prescribes a selection of allowable metal linewidth and spacing rules for same and different metal colors (for double or multiple-layer patterning). Figure 5 contains a sample table of allowable combinations of metal width and spacing created in this way. At the expense of minimal additional complexity, prescriptive design allows for rules to be defined with higher confidence, making for larger, more predictable process windows.

Templated design is an approach to avoiding overly restrictive design rules and design methodologies. The introduction of template libraries can help to reduce the occurrence of design-process interactions that can limit critical process windows (for which a single weak point can create severe yield issues if present at high instance rates, as shown in Figure 6). Templates limit utilization of unique layout patterns and special constructs, allowing for full characterization of the logic layout space. Templates also provide a controlled environment for faster design library development, leading to known process windows and shorter time to yield and volume ramp. However, the use of templates mandates an upfront design approach and can lead to significant area penalties.

2.2 Materials
In addition to various design approaches, several new metallic and dielectric materials have become available to expand overall windows within unit process itself. Implementation of CVD cobalt liner and capping layers (as evidenced in Figure 7) has been shown to dramatically improve Cu seed wetting and seed nucleation versus traditional PVD TaN/Ta alone. Figure 8 shows representative, comparative images with and without insertion of Co liner both after initial plated Cu[11] and as fully-integrated (post-CMP) in M1 islands. Co liner has been shown to improve Cu adhesion during the simultaneous dep-etch PVD seed
process, resulting in greatly increased seed coverage in high-aspect ratio trenches and in trenches with non-ideal or undercut sidewall profiles – which in turn leads to improved void-free Cu fill. Integration of a post-CMP Co capping layer has been further shown to greatly enhance resistance to Cu electromigration over conventional and alternative[2] metallic diffusion barriers. Co capping layers can be integrated with other CVD liner materials such as ruthenium, which further enables reflow of Cu during seed deposition[3] – again greatly improving void-free metal fill (as evidenced in Figures 9 and 10, respectively). CVD liners such as Co and Ru allow for improved seed coverage over increasingly porous (e.g. lower and lower dielectric constant materials) sidewalls, and may additionally allow for reduced barrier thickness (enabling improved RC performance).

New dielectric materials and the incorporation of advanced dielectric capping layers also serve to enlarge integrated process windows. Improvements in both mechanical strength and resistance to process-induced damage for new dielectric materials (shown in Figure 11) have made overall integrations less-sensitive to hard mask undercut (which limits yield) and more resistant to plasma (which improves RC performance by reducing integrated dielectric constant). Advanced dielectric capping materials to replace or complement SiCN allow for improved aspect ratios (and thereby enhanced process window) through continued physical thickness scaling and improved etch selectivity. Figure 12 highlights cumulative improvement in integrated via aspect ratios for incremental improvements in hard mask removal and with advanced capping materials.

2.3 Integration

Progression to sub-30nm linewidths requires that the incumbent LELE (Litho-Etch-Litho-Etch) patterning process integration either be extended to LELELE (through yet an additional Litho-Etch sequence) or to novel SADP (Self-Align Deserted Pattern) or SAQP (Self-Align Quadruple Pattern). Figures 13 and 14 show schematic comparisons of LELELE/SADP and SADP/SAQP integrations.[4] While both LELELE and SADP/SAQP are feasible, LELELE requires exceedingly tight overlay performance (i.e. multiple alignments in this scheme combine to severely limit process window). Alternatively, SADP opens up overlay process window for tight-pitch metals, but success with this integration hinges upon mandrel/spacer material selection - and requires high-throughput deposition and etch processes. Pitch quadrupling (SAQP) further opens process window in lithography through improved within-field and within-wafer uniformity, though SAQP also depends heavily upon precise control of thin film thickness variation.

3. Summary

Many individual approaches to BEOL process window expansion have been identified in order to enable continued BEOL scaling into sub-30nm critical dimensions. While each of these individual improvements are indeed necessary, none are alone sufficient - nor do they come without added complexity or cost. Successful realization of process window enlargement requires proactive co-optimization each from design, process, and process integration as an integral part of up-front technology planning.

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References

Fig. 1 Normalized Monte Carlo simulations for a 64nm-pitch via integrated to full theoretical process assumptions, for the same via upsized for optimal yield and/or performance, and with maximal additional in-line control.

Fig. 2 Product-level limited yield window between opens and shorts for systematic design weak points a) before and b) after simultaneous design and process optimization.

Fig. 3 Sample layout clips for a) largely unrestricted, b) partially-restricted, and c) more-restricted router configurations.

Fig. 4 Sample Line End Extension (LEE) statistics as a function of router properties.

Fig. 5 Sample table of simulated allowable combinations of metal width and spacing for same and different colors (for double or multiple-layer patterning).

Fig. 6 Limited yield as a function of sample weak point failure rate.

Fig. 7 Cross-sectional TEM and corresponding EDX images of integrated Co liner and Co capping layers.
Fig. 8 Representative comparative images with and without insertion of Co liner after a) 4nm plated Cu [nucleation], and b) post-CMP in M1 islands.

Fig. 9 Top-down images (post-CMP) comparing impact of Ru liner/Cu reflow upon void formation.

Fig. 10 EDX maps demonstrating Ru liner integration with Co cap, with schematic and XTEM image of Cu reflow enabled by Ru liner.

Fig. 11 Table of bulk dielectric constant, modulus, and Process-Induced Damage for 5 ILD materials, highlighting impact on relative patterning process window.

Fig. 12 Schematic of cumulative improvement in integrated via Aspect Ratio (AR) for incremental improvements in hard mask removal and with advanced capping materials.

Fig. 13 Schematic comparison of Litho-Etch-Litho-Etch-Litho-Etch (LELELE) and Self-Aligned Double Patterning (SADP).

Fig. 14 Schematic comparison of SADP (Self-Aligned Double Patterning) and SAQP (Self-Aligned Quadruple Patterning) integrations.